SONY CXK5816PN/M 10/10L/12/12L/15/15L

2K-word × 8 bit High Speed CMOS Static RAM

Description

The CXK5816PN/M is a 16,384 bits high speed CMOS static RAM organized as 2,048 words by 8 bits and operates from a single 5V supply. The CXK5816PN/M is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Low power standby: 5μW(Typ.)—L-version
  100μW(Typ.)—Standard version
- Low power operation: 125mW(Typ.)
- Fast access time: 100ns/120ns/150ns (Max.)
- Single +5V supply
- Fully static memory ..... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: 3-state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Pin compatible with MB8416A, HM6116, μPD446

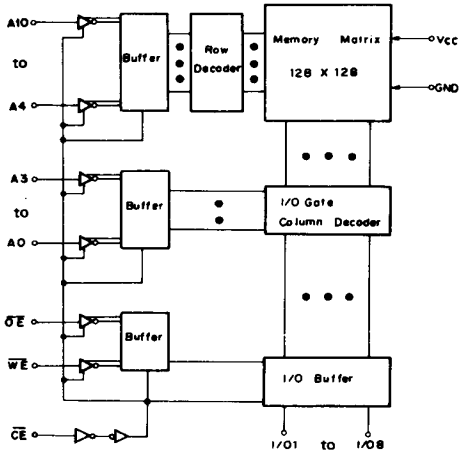
Structure

Silicon gate CMOS IC

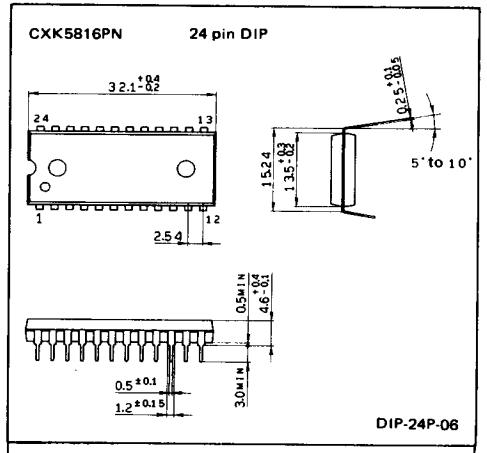
Function

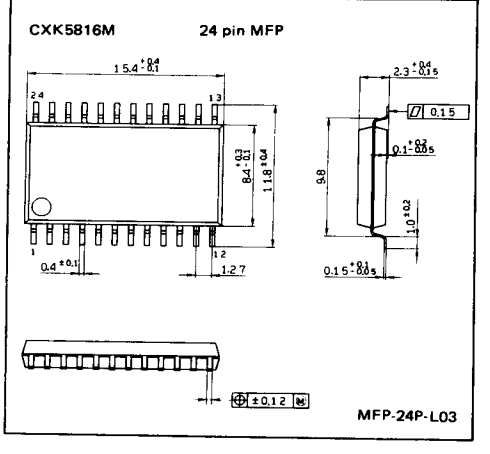
2048-word × 8 bit static RAM

Block Diagram



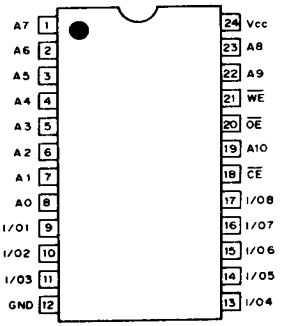
Package Outline Unit: mm





Note) All Typical values are measured under the conditions Vcc=5.0V and Ta=25°C.

Pin Configuration (Top View)



Symbol	Description
A0 to A10	Address Input
I/O1 to I/O8	Data Input Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply Voltage	V_{CC}		−0.5 to +7.0	V
Input Voltage	V_{IN}		−0.5 to V_{CC}+0.5	V
Input and Output Voltage	$V_{I/O}$		−0.5 to V_{CC}+0.5	V
Allowable Power Dissipation	P_D	CXK5816PN	1.0	W
		CXK5816M	0.7	
Operating Temperature	Topr		0 to +70	°C
Storage Temperature	Tstg		−55 to +150	°C
Soldering Temperature	Tsolder		260 • 10	°C • sec

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not Selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output Disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	D out	I_{CC1}, I_{CC2}
L	X	L	Write	D in	I_{CC1}, I_{CC2}

Note) X: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V

DC and Operating Characteristics

(V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test condition	CXK5816PN/M −10/12/15			CXK5816PN/M −10L/12L/15L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN}=GND to V_{CC}	−2	—	2	−2	—	2	μA
Output Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	−2	—	2	−2	—	2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}=V_{IL}$, I_{OUT}=0mA	—	—	60	—	—	60	mA
Average Operating Current	I_{CC2}	Cycle = Min, Duty = 100% I_{OUT}=0mA	—	28 *(31)	60 *(75)	—	28 *(31)	60 *(75)	mA
Standby Current	I_{SB1}	$\overline{CE}\geq V_{CC}-0.2V$	—	—	1.0	—	—	0.05	mA
	I_{SB2}	$\overline{CE}=V_{IH}$	—	—	2	—	—	1	mA
Output High Voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	2.4	—	—	V
Output Low Voltage	V_{OL}	$I_{OL}=4.0mA$	—	—	0.4	—	—	0.4	V

Note) * Shows CXK5816PN/M-10, 10L value.

Capacitance

(Ta=25°C, f=1 MHz)

Item	Test condition	Symbol	Min.	Max.	Unit
Input Capacitance	V_{IN}=0V	C_{IN}	—	7	pF
Input/Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$	—	10	pF

Note) This parameter is sampled and is not 100% tested.

AC Operating Characteristics

- **AC Test condition**

(V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Item	Condition
Input Pulse High Level	$V_{IH}=2.4V$
Input Pulse Low Level	$V_{IL}=0.6V$
Input Rise Time	t_R = 5ns
Input Fall Time	t_F = 5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L* = 100pF, 1TTL

* C_L includes scope and jig capacitance.

Read Cycle

Item	Symbol	CXK5816PN/M -10/10L		CXK5816PN/M -12/12L		CXK5816PN/M -15/15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100	—	120	—	150	—	ns
Address Access Time	t_{AA}	—	100	—	120	—	150	ns
Chip Enable Access Time ($\overline{CE}$)	t_{CO}	—	100	—	120	—	150	ns
Output Enable to Output Valid	t_{OE}	—	50	—	55	—	60	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	15	—	ns
Chip Enable to Output in Low Z ($\overline{CE}$)	t_{LZ}	15	—	15	—	15	—	ns
Output Enable to Output in Low Z ($\overline{OE}$)	t_{OLZ}	10	—	10	—	10	—	ns
Chip Disable to Output in High Z	*t_{HZ}	0	30	0	40	0	50	ns
Output Disable to Output in High Z ($\overline{OE}$)	*t_{OHZ}	0	30	0	40	0	50	ns

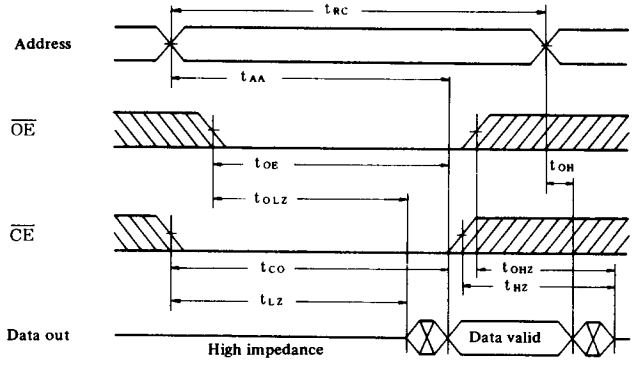
* t_{HZ} and t_{OHZ} are specified by the time length when the output circuit becomes closed and not specified by the output voltage level.

Write Cycle

Item	Symbol	CXK5816PN/M -10/10L		CXK5816PN/M -12/12L		CXK5816PN/M -15/15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	100	—	120	—	150	—	ns
Address Valid to End of Write	t_{AW}	80	—	100	—	120	—	ns
Chip Enable to End of Write	t_{CW}	80	—	100	—	120	—	ns
Data to Write Time Overlap	t_{DW}	30	—	35	—	40	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	60	—	75	—	90	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	5	—	ns
Output Active from End of Write	t_{OW}	15	—	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	30	0	40	0	50	ns

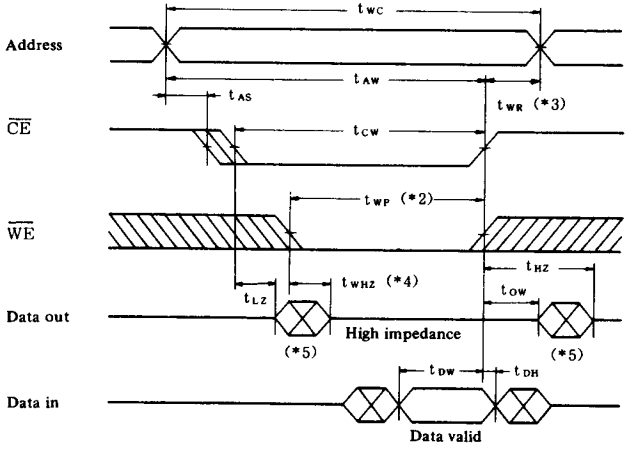
Timing Waveform

(1) Read Cycle [$\overline{WE}$=V_{IH}]

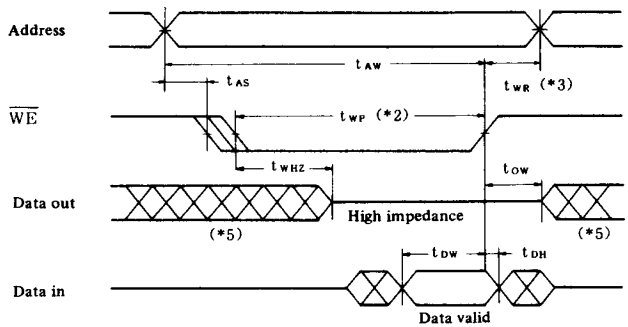


(2) Write Cycle

- **Write Cycle No. 1: [$\overline{OE}$=V_{IL} or V_{IH}] (*1)**



• Write Cycle No. 2: [$\overline{OE}$=V_{IL} or V_{IH}, $\overline{CE}$=V_{IL}] (*1)



*** Note)**

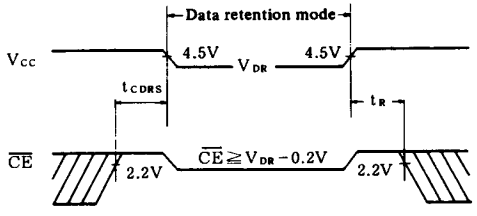
1. If $\overline{OE}$ is high, output remains in a high impedance state.
2. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
4. If $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Data Retention Characteristics (Ta = 0 to +70 °C)

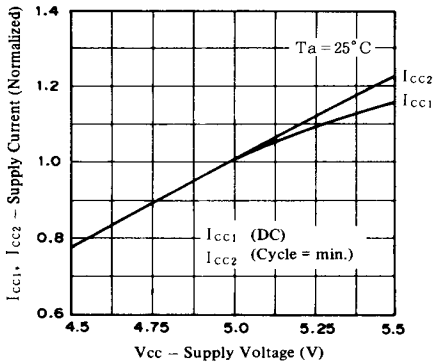
Item	Symbol	Test condition	CXK5816PN/M −10/12/15			CXK5816PN/M −10L/12L/15L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data Retention Voltage	V_{DR}	$\overline{CE} \geqq V_{CC} - 0.2V$	2.0	—	5.5	2.0	—	5.5	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0V$, $\overline{CE} \geqq 2.8V$	—	—	600	—	—	30	μA
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$, $\overline{CE} \geqq V_{CC} - 0.2V$	—	—	1000	—	—	50	μA
Data Retention Set up Time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery Time	t_R		t_{RC}*	—	—	t_{RC}*	—	—	ns

* t_{RC} : Read Cycle Time

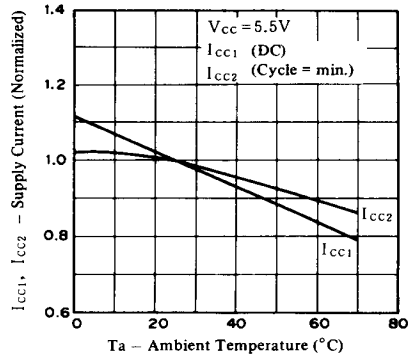
Data Retention Waveform



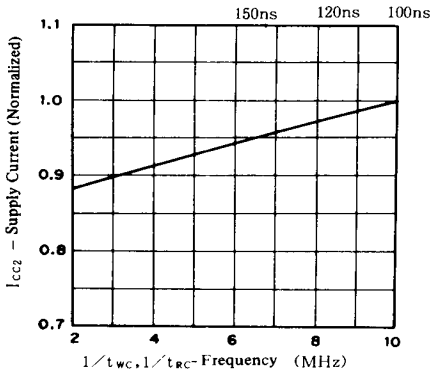
Supply Current vs. Supply Voltage



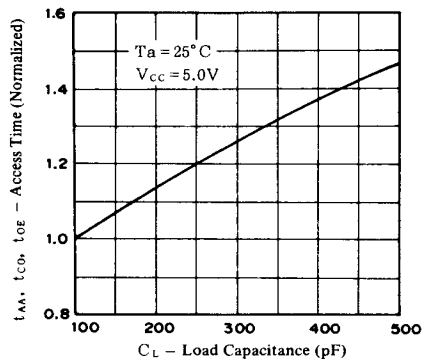
Supply Current vs. Ambient Temperature



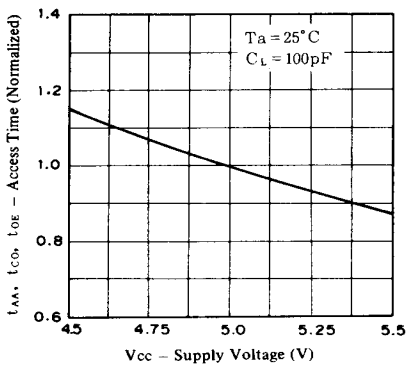
Supply Current vs. Frequency



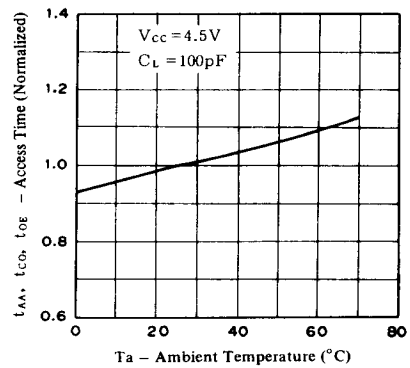
Access Time vs. Load Capacitance



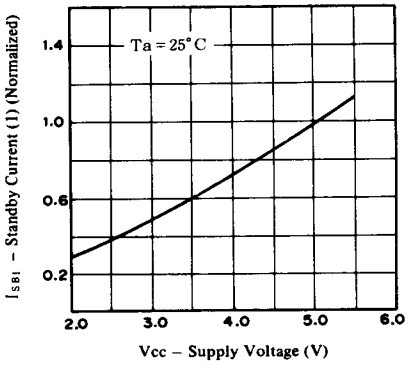
Access Time vs. Supply Voltage



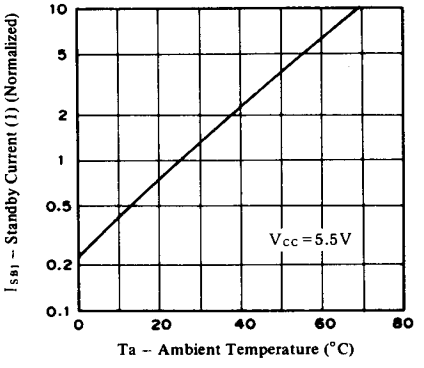
Access Time vs. Ambient Temperature



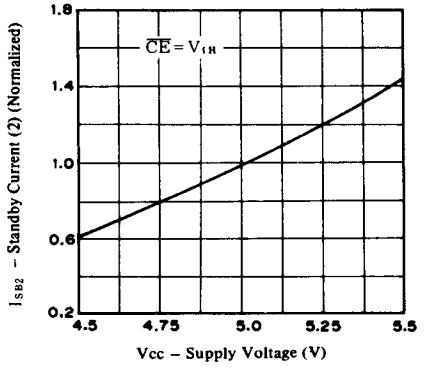
Standby Current (1) vs. Supply Voltage



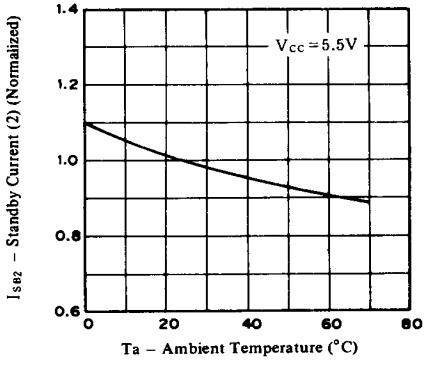
Standby Current (1) vs. Ambient Temperature



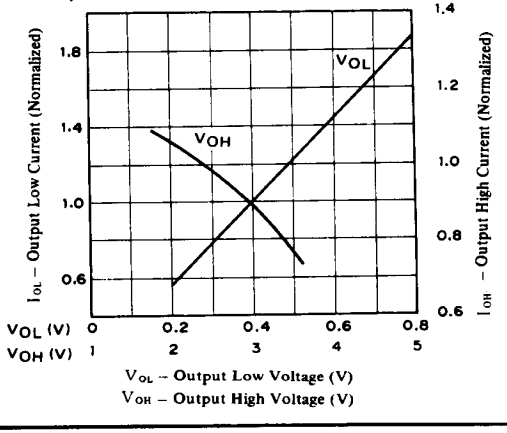
Standby Current (2) vs. Supply Voltage



Stadby Current (2) vs. Ambient Temperature



Output High Current vs. Output High Voltage
Output Low Current vs. Output Low Voltage



Input Voltage vs. Supply Voltage