

# DATA SHEET

## **J210; J211; J212** N-channel field-effect transistors

Product specification  
File under Discrete Semiconductors, SC07

1997 Dec 01

# N-channel field-effect transistors

# J210; J211; J212

### FEATURES

- High speed switching
- Interchangeability of drain and source connections
- High impedance.

### APPLICATIONS

- Analog switches
- Choppers, multiplexers and commutators
- Audio amplifiers.

### DESCRIPTION

N-channel symmetrical junction field-effect transistor in a TO-92 (SOT54) package.

<b>CAUTION</b>
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

### PINNING - TO-92 (SOT54)

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

*MAM197*

**Marking codes:**  
 J210: J210.  
 J211: J211.  
 J212: J212.

Fig.1 Simplified outline and symbol.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	±25	V
$V_{GSoff}$	gate-source cut-off voltage	$I_D = 1 \text{ nA}; V_{DS} = 15 \text{ V}$			
	J210		–1	–3	V
	J211		–2.5	–4.5	V
	J212		–4	–6	V
$I_{DSS}$	drain current	$V_{GS} = 0; V_{DS} = 15 \text{ V}$			
	J210		2	15	mA
	J211		7	20	mA
	J212		15	40	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 50 \text{ °C}$	–	400	mW
$ y_{fs} $	common-source transfer admittance	$V_{GS} = 0; V_{DS} = 15 \text{ V}$			
	J210		4	12	mS
	J211		6	12	mS
	J212		7	12	mS

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		–	±25	V
V <sub>GSO</sub>	gate-source voltage	open drain	–	–25	V
V <sub>DGO</sub>	drain-gate voltage	open source	–	–25	V
I <sub>G</sub>	forward gate current (DC)		–	10	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 50 °C; note 1; see Fig.13	–	400	mW
T <sub>stg</sub>	storage temperature		–65	150	°C
T <sub>j</sub>	operating junction temperature		–	150	°C

**Note**

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm<sup>2</sup>.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient; note 1	250	K/W

**Note**

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm<sup>2</sup>.

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## STATIC CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = -1\ \mu\text{A}; V_{DS} = 0$	–	–25	V
$V_{GSoff}$	gate-source cut-off voltage	$I_D = 1\ \text{nA}; V_{DS} = 15\ \text{V}$			
	J210		–1	–3	V
	J211		–2.5	–4.5	V
	J212		–4	–6	V
$V_{GSS}$	gate-source forward voltage	$I_G = 0; V_{DS} = 0$	–	1	V
$I_{DSS}$	drain current	$V_{GS} = 0; V_{DS} = 15\ \text{V}$			
	J10		2	15	mA
	J11		7	20	mA
	J12		15	40	mA
$I_{GSS}$	reverse gate leakage current	$V_{GS} = -15\ \text{V}; V_{DS} = 0$	–	–100	pA
$ y_{fs} $	common-source transfer admittance	$V_{GS} = 0; V_{DS} = 15\ \text{V}$			
	J210		4	12	mS
	J211		6	12	mS
	J212		7	12	mS
$ y_{os} $	common source output admittance	$V_{GS} = 0; V_{DS} = 15\ \text{V}$			
	J210		–	150	$\mu\text{S}$
	J211		–	200	$\mu\text{S}$
	J212		–	200	$\mu\text{S}$

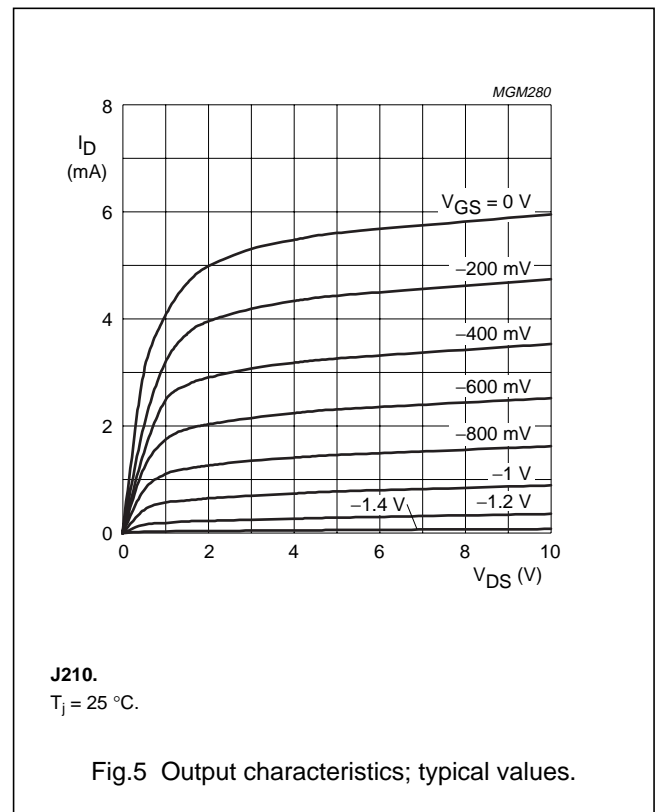
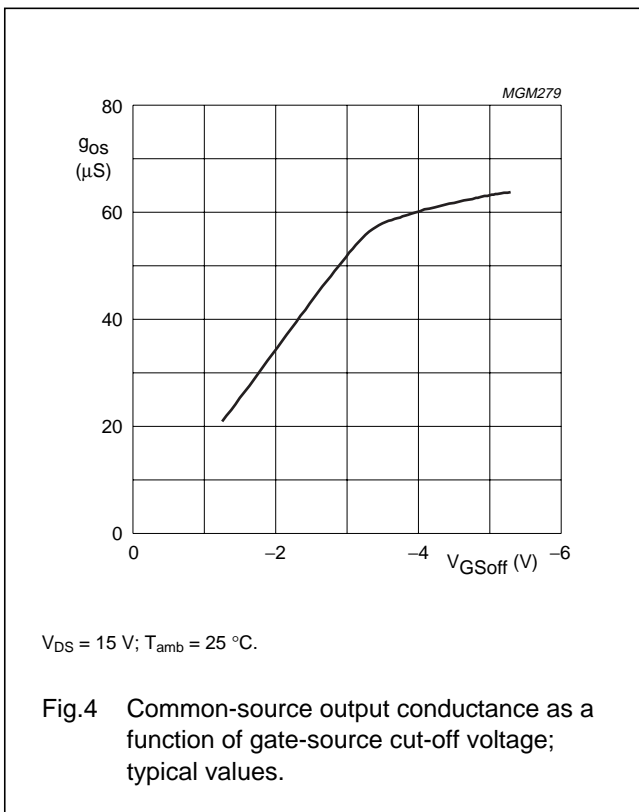
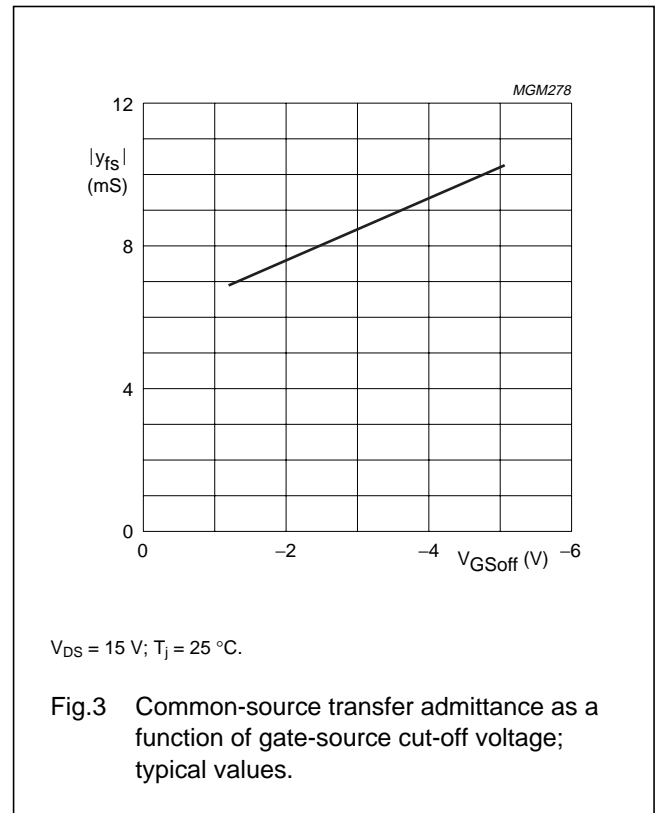
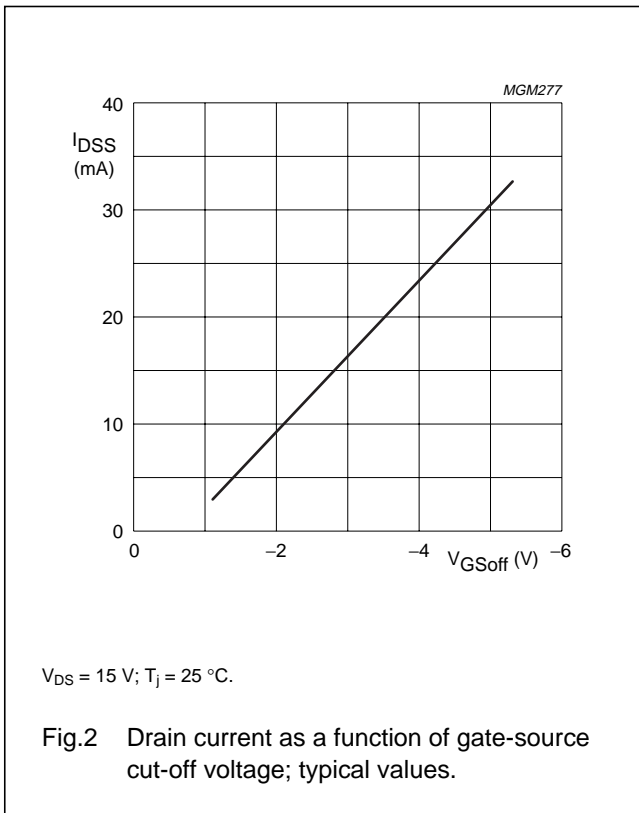
## DYNAMIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
$C_{is}$	input capacitance	$V_{DS} = 15\ \text{V}; V_{GS} = -10\ \text{V}; f = 1\ \text{MHz}$	2	pF
		$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	4	pF
$C_{os}$	output capacitance	$V_{DS} = 15\ \text{V}; V_{GS} = -10\ \text{V}; f = 1\ \text{MHz}$	0.8	pF
		$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	2	pF
$C_{rs}$	feedback capacitance	$V_{DS} = 15\ \text{V}; V_{GS} = -10\ \text{V}; f = 1\ \text{MHz}$	0.8	pF
		$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	0.9	pF
$g_{is}$	common source input conductance	$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 100\ \text{MHz}$	70	$\mu\text{S}$
		$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 450\ \text{MHz}$	1.1	mS
$g_{fs}$	common source transfer conductance	$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 100\ \text{MHz}$	7.5	mS
		$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 450\ \text{MHz}$	7.5	mS
$g_{rs}$	common source feedback conductance	$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 100\ \text{MHz}$	–8	$\mu\text{S}$
		$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 450\ \text{MHz}$	–90	$\mu\text{S}$
$g_{os}$	common source output conductance	$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 100\ \text{MHz}$	95	$\mu\text{S}$
		$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 450\ \text{MHz}$	200	$\mu\text{S}$
$V_n$	equivalent input noise voltage	$V_{DS} = 15\ \text{V}; V_{GS} = 0; f = 1\ \text{kHz}$	5	nV/ $\sqrt{\text{Hz}}$

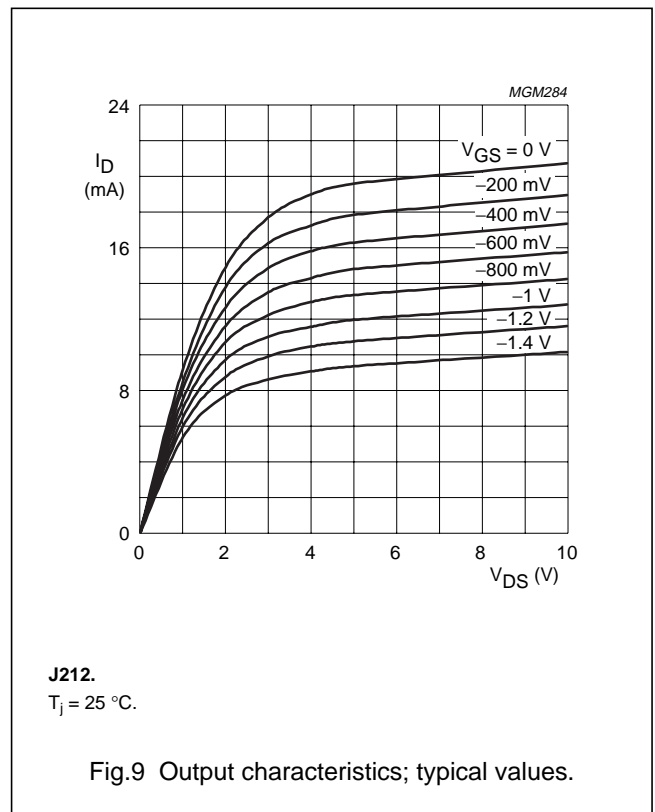
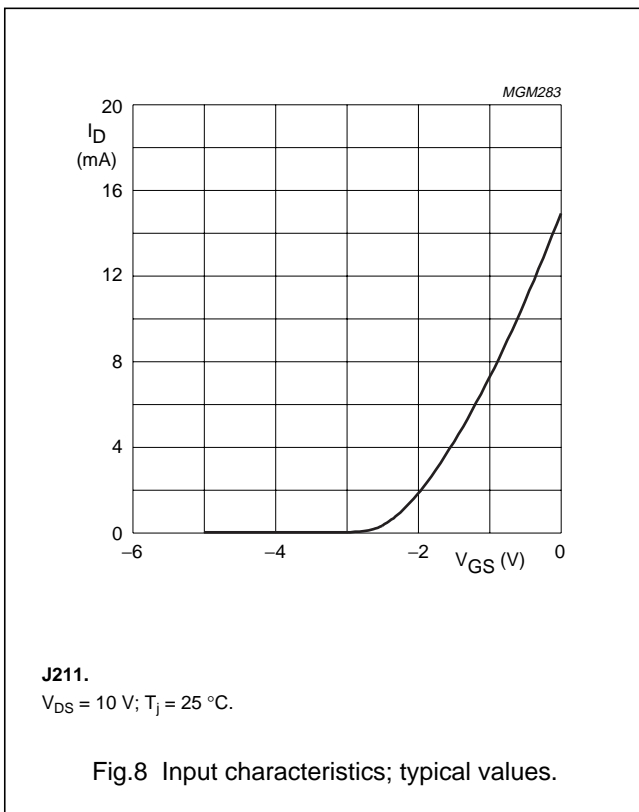
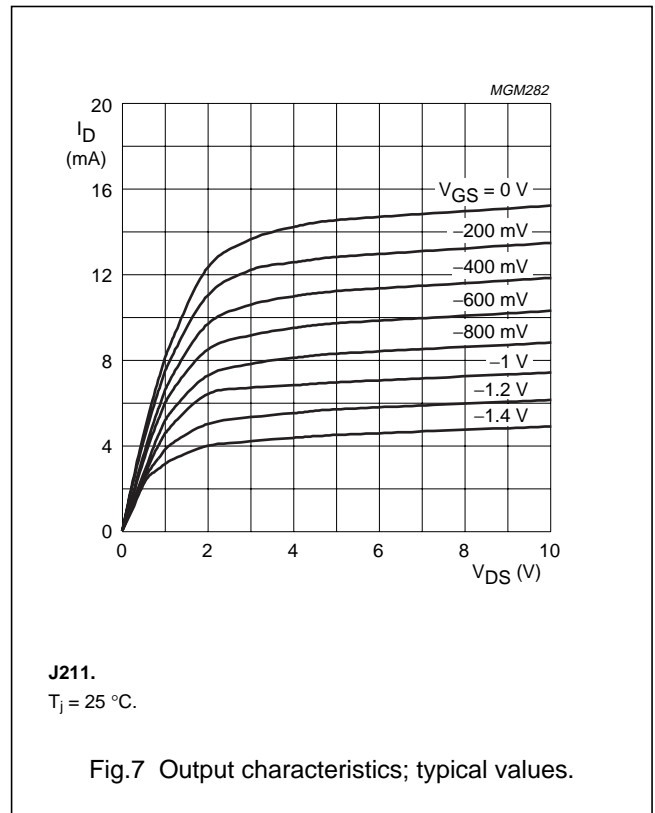
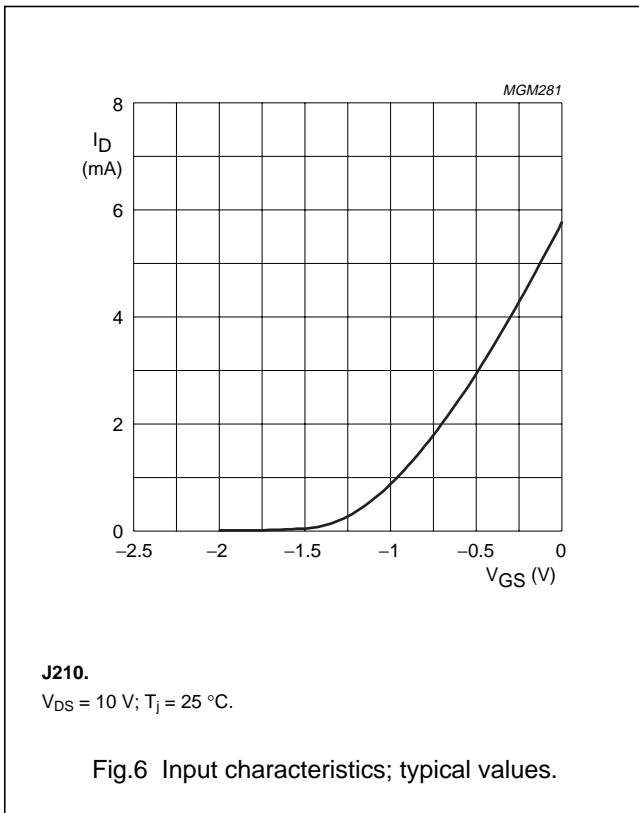
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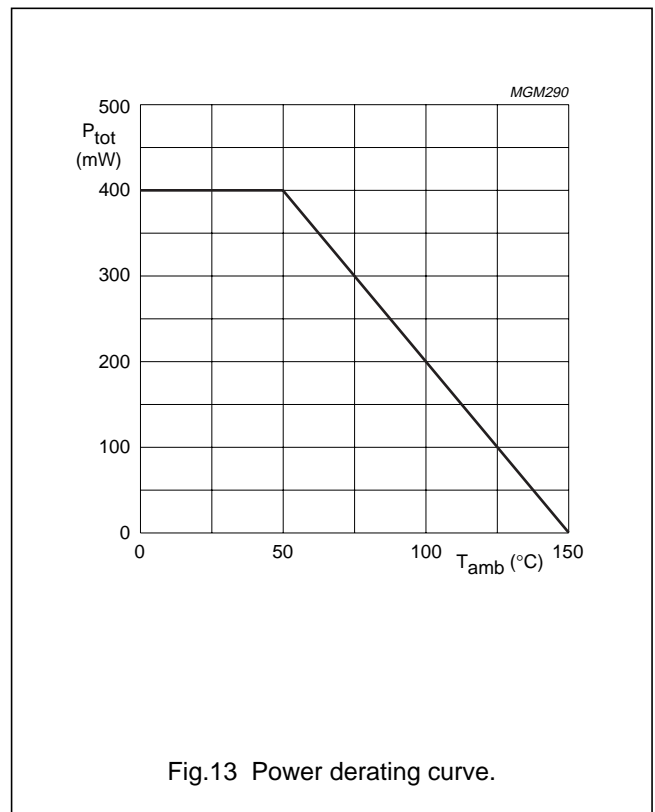
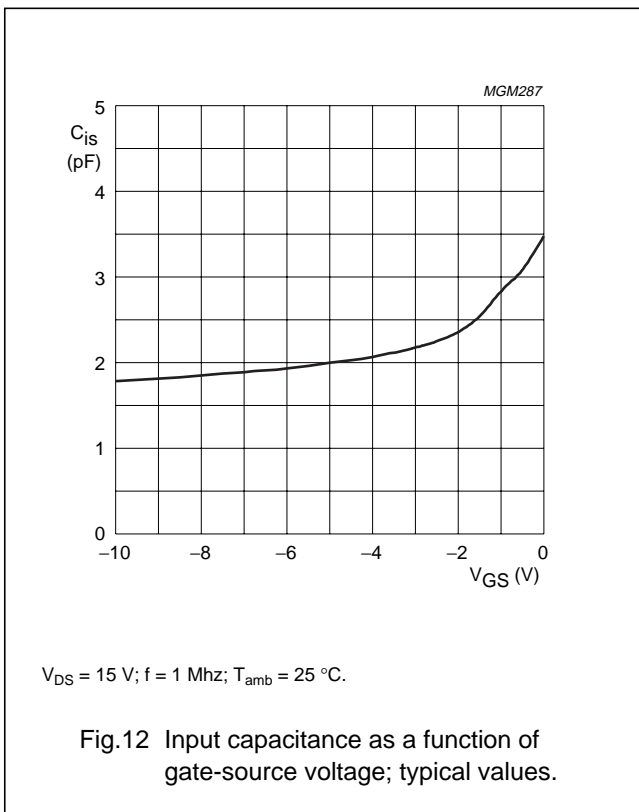
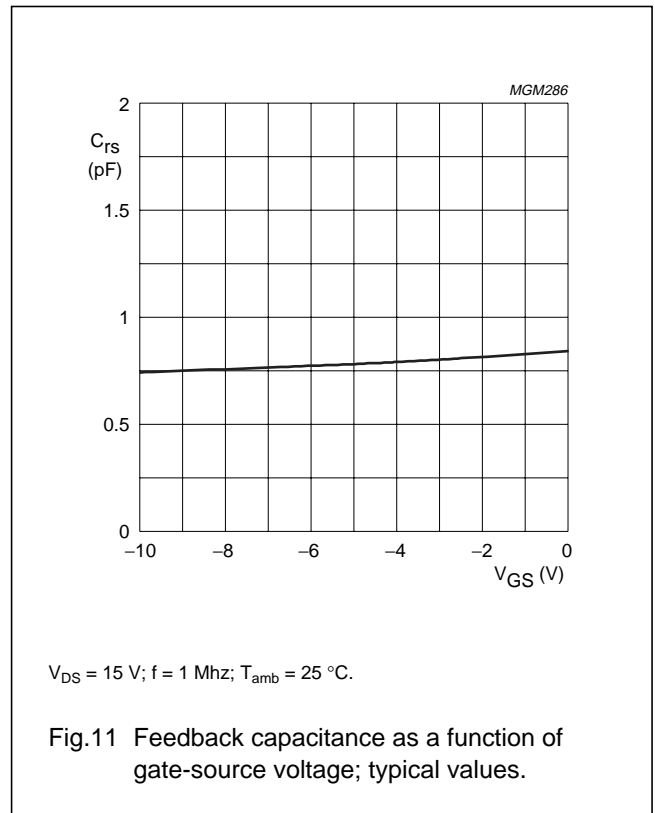
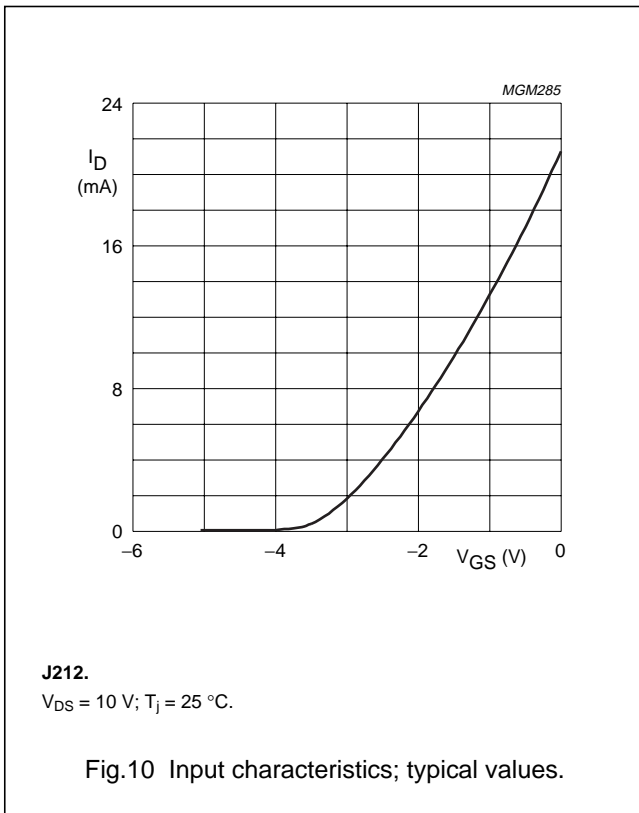
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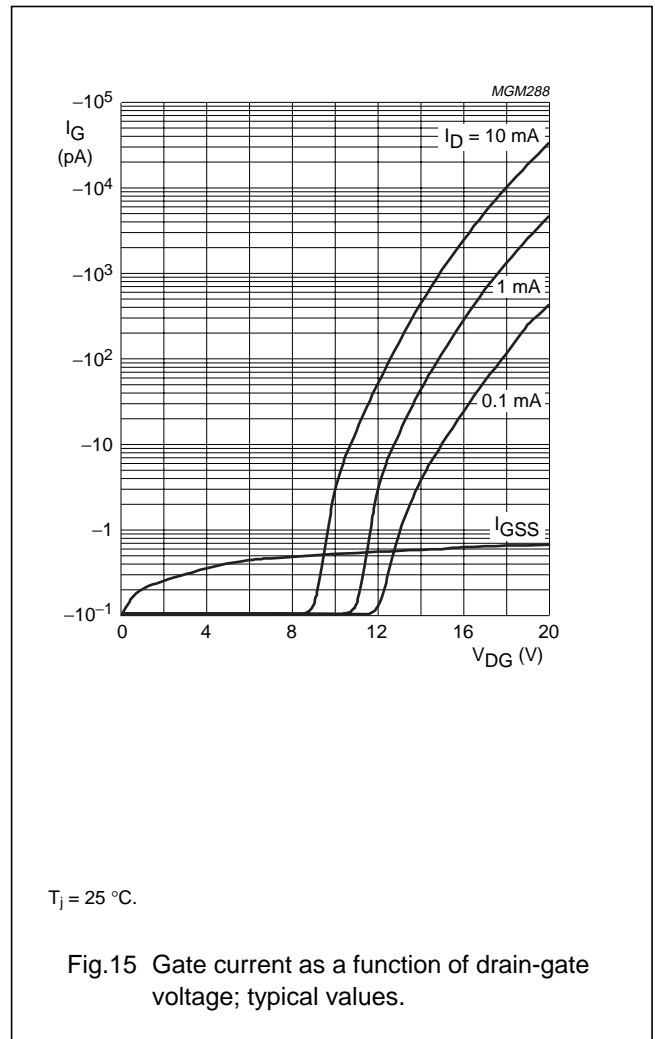
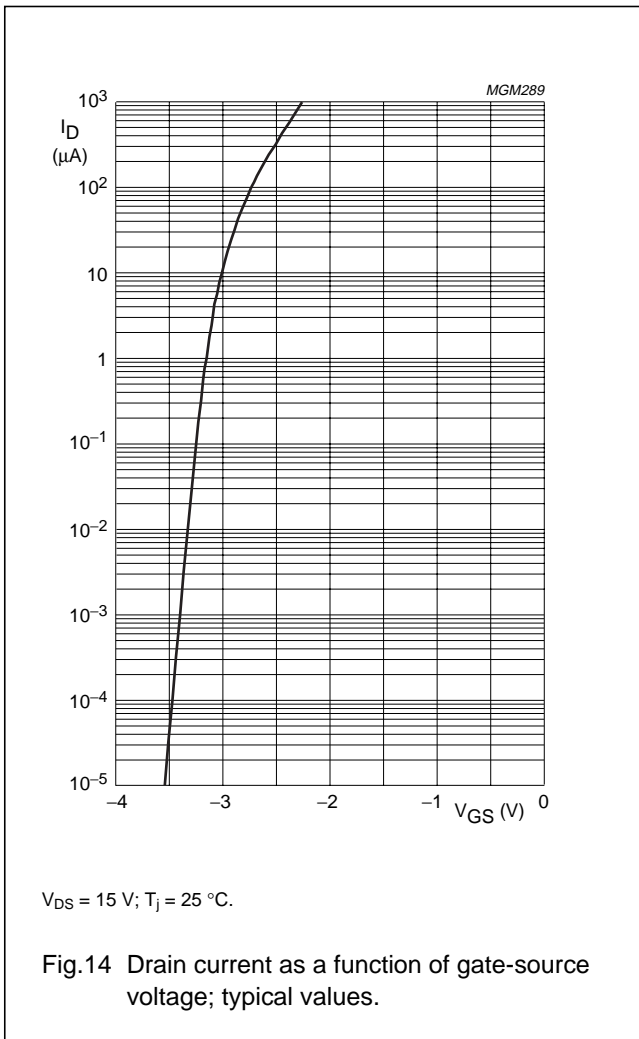
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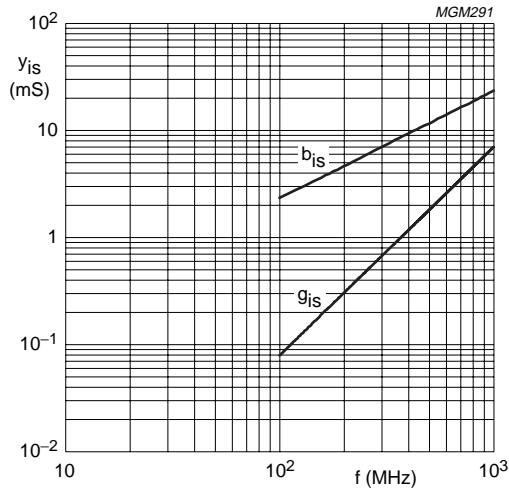
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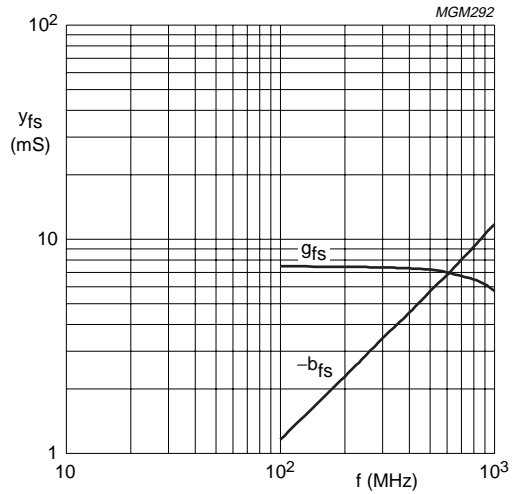
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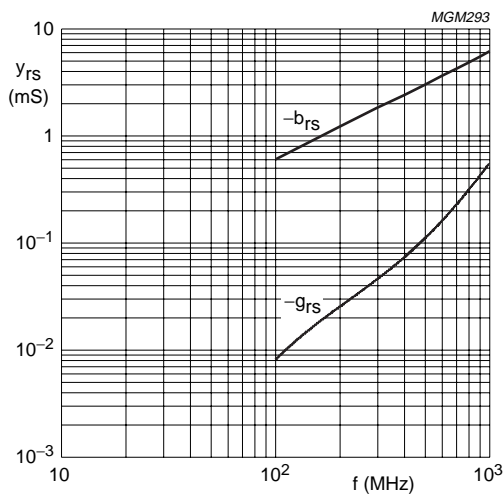
$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}.$

Fig.16 Common source input admittance as a function of frequency; typical values.



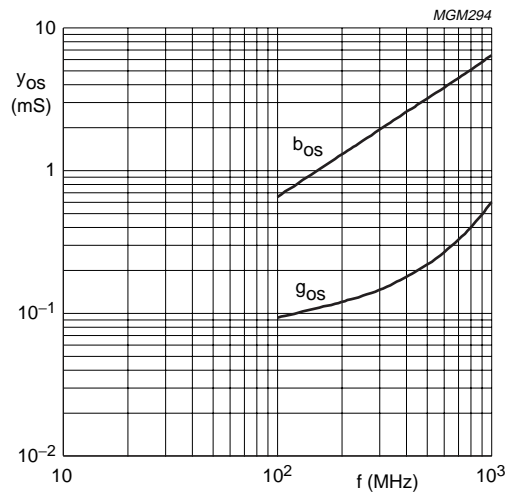
$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}.$

Fig.17 Common source transfer admittance as a function of frequency; typical values.



$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}.$

Fig.18 Common source reverse admittance as a function of frequency; typical values.



$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^\circ\text{C}.$

Fig.19 Common source output admittance as a function of frequency; typical values.

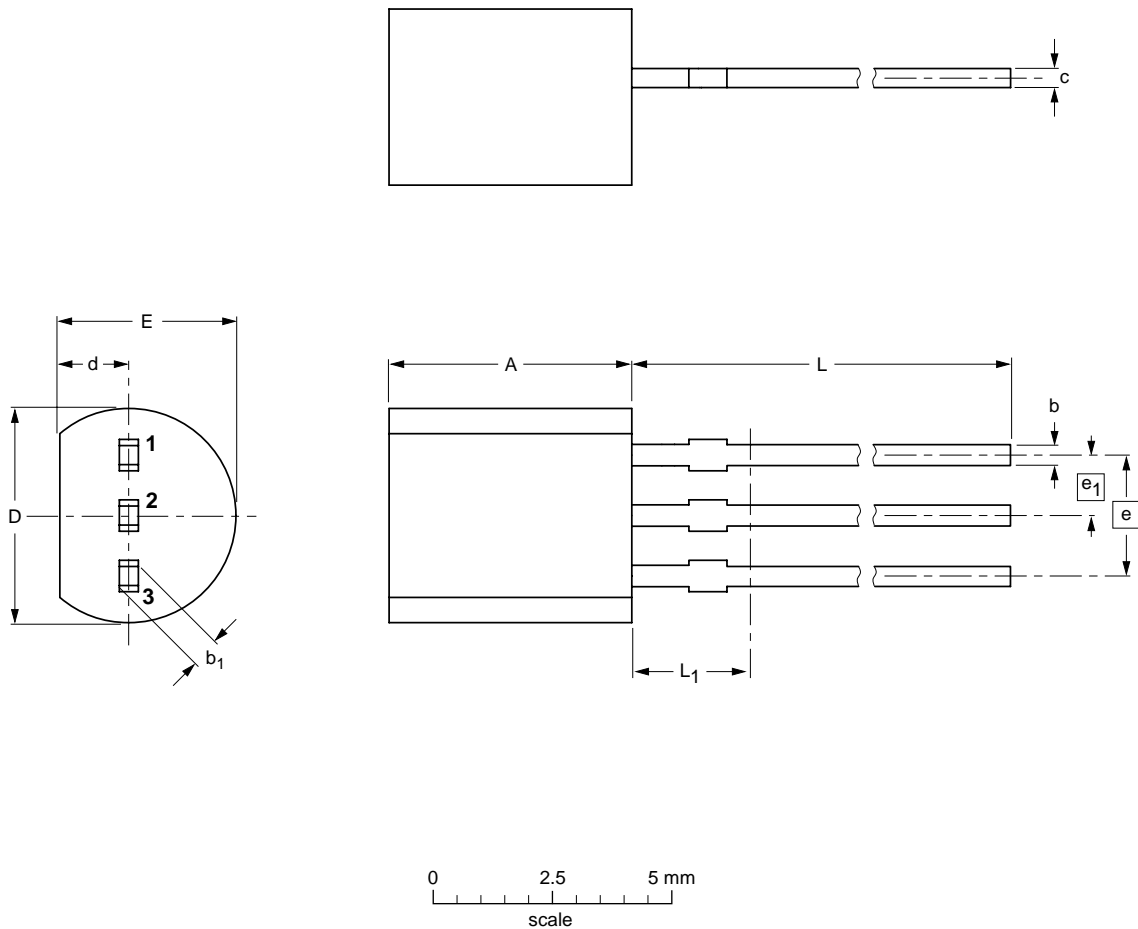
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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup>
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54		TO-92	SC-43		97-02-28

## N-channel field-effect transistors

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**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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