4,096 WORD X 8 BIT MASK ROM

N-CHANNEL SILICON GATE

TMM2332P

DESCRIPTION

The TMM2332P is a 32768-bit read only memory organized as 4096 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using microprocessor.

The TMM2332P features an automatic power down mode. When deselected by Chip Select (CS/$\overline{CS}$), the device is in low power (I_{SB}=15mA MAX.) standby mode. This device feature results in system power saving in larger systems, where the majority of devices are deselected.

The TMM2332P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance.

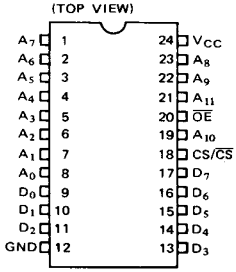
The TMM2332P is moulded in a 24-pin standard plastic package.

FEATURES

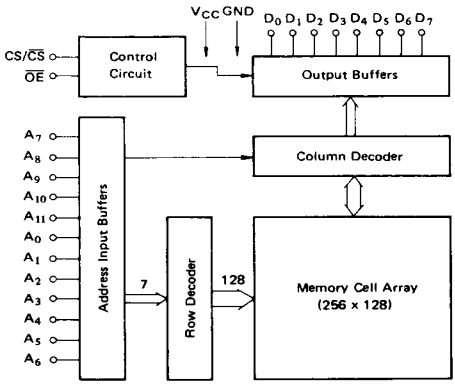
- Single 5V-Power Supply
- Fast Access Time: 350ns (MAX.)
- Low Power Dissipation
  - Operating Current = 100mA (MAX.)
  - Standby Current = 15mA (MAX.)
- Power Down Feature: CS / $\overline{CS}$
- Programmable Chip Select: CS / $\overline{CS}$
- Output Buffer Control : $\overline{OE}$
- Easy memory Expansion : CS / $\overline{CS}$
- Static Operation
- Pin Compatible with 2732 Type EPROM and i2332
- All Inputs and Outputs:
  - Directly TTL Compatible
- Three State Outputs: Wired OR Capability.
- Inputs Protected: All inputs have protection against static charge.

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{11}	Address Inputs
D_0~D_7	Data Outputs
CS/$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-0.5 ~ 7.0	V
V_{OUT}	Output Voltage	-0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{SOLDER}	Soldering Temperature·Time	260 · 10	°C·Sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.5	–	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

D.C. CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{CC}	–	±0.02	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-0.4	-2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	4.0	–	mA
I_{LO}	Output Leakage Current	$\overline{OE}$ = V_{IH} or $\overline{CS}$ = V_{IH} V_{OUT} = 0.4V ~ V_{CC}	–	±0.05	±10	μA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL} or CS = V_{IH}	–	–	100	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH} or CS = V_{IL}	–	–	15	mA

CAPACITANCE (T_a = 0 ~ 70°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	8	15	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

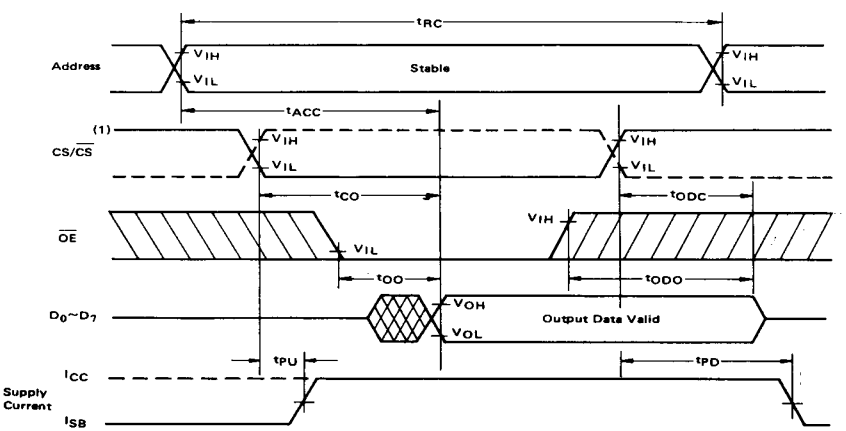
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	350	–	–	ns
t_{ACC}	Access Time	–	–	350	ns
t_{CO}	Chip Selection to Output Valid	–	–	350	ns
t_{OO}	$\overline{OE}$ to Output Valid	–	–	120	ns
t_{ODC}	Chip Deselection to Output in High-Z	–	–	100	ns
t_{ODO}	$\overline{OE}$ to Output in High-Z	–	–	100	ns
t_{PU}	Chip Selection to Power Up Time	0	–	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	–	100	ns

A.C. TEST CONDITIONS

Input Rise and Fall Times ; 20ns
Timing Measurement Reference Levels ; Input : 0.8V and 2.0V
Output: 0.8V and 2.0V

Output Load; 1-TTL Gate and C_L = 100pF

A.C. TIMING WAVEFORMS

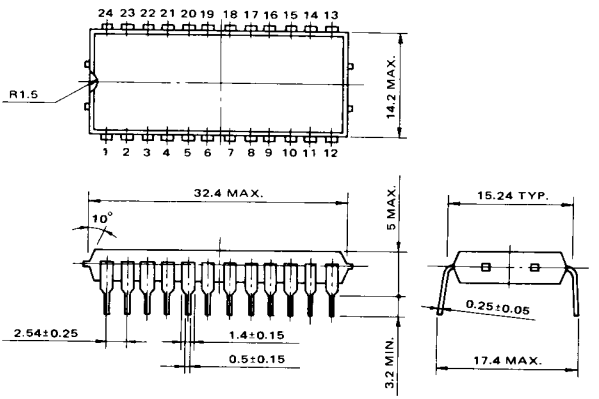


Note: (1) CS and $\overline{CS}$ waveforms are shown by dotted line and straight line respectively.

ACCEPTABLE FORMAT

Toshiba can accept programming and masking information for TMM2332P in the form of punched paper tape with Intel BNPF format or master devices (EPROM).

OUTLINE DRAWINGS



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm longitudinal position with respect to No. 1 and No. 24 leads. All dimensions are in millimeters.