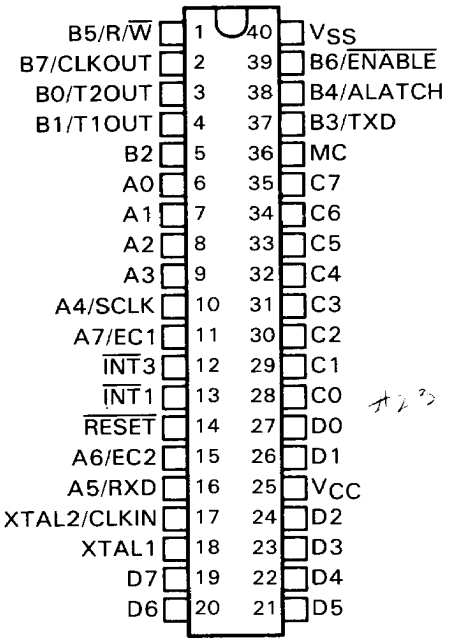
# TMS70C42/TMS70C02
# 8-BIT CMOS MICROCOMPUTERS

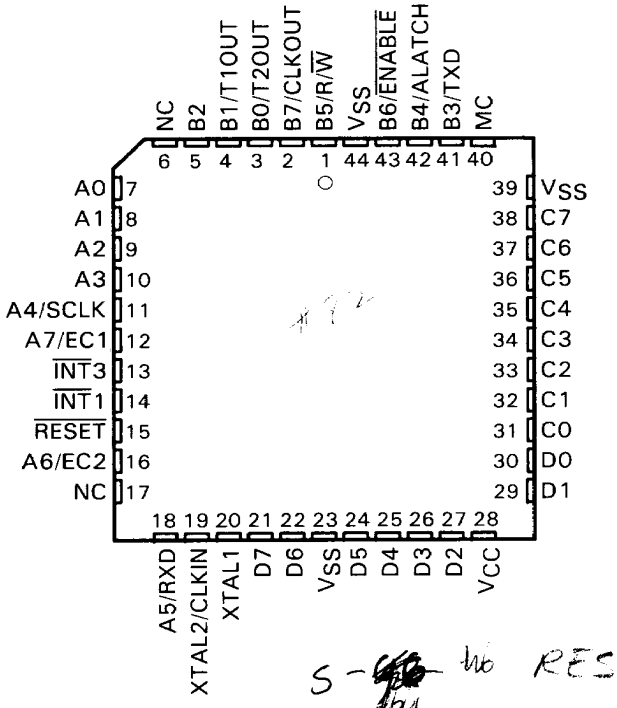
APRIL 1986

- CMOS Technology
- Wide Operating Range
  - Voltage ($V_{CC}$) 2.5 V to 6.0 V
  - Frequency 0.5 MHz to 6.0 MHz
  - Temperature −40°C to 85°C
- Low Operating Current
  - 15 mA Typical Operating Current at 6 MHz
  - Wake-Up Mode for Power Savings
- Flexible Memory Configurations
  - 256-Byte On-Chip RAM Register File
  - Memory-Mapped Ports for Easy Addressing
  - 4K-Byte On-Chip ROM (TMS70C42)
  - Memory Expansion to 64K Bytes
- TMS70C02 ROMless Microprocessor
- 32 CMOS Compatible I/O Pins (TMS70C42)
  - 24 Bidirectional Pins
  - 8 Output Pins
- Three On-Chip Timers:
  - Two 16-Bit with 5-Bit Prescale and 16-Bit Capture Latch, Cascadable
  - Timer Outputs on Timer 1 and Timer 2
  - One 8-Bit with 2-Bit Prescale
  - Internal Interrupt with Automatic Timer Reload
- On-Chip Serial Port
  - Flexible Data Protocols
  - Internal or External Baud Rate Generator
  - Error Detection Flags
  - Separate Baud Rate Generator or Usable as a Third General Purpose Timer
  - Asynchronous, Synchronous, and Serial Modes
  - Two Multiprocessor Communication Formats
- Flexible Interrupt Handling:
  - External Interrupts Programmable for Edge or Edge/Level Triggering
  - External Interrupts Programmable for Rising or Falling Edge Detection
  - Software Calls through Interrupt Vectors
  - Software Monitoring of Interrupt Status
  - Precise Interrupt Timing through Capture Latch
  - Priority Servicing of Simultaneous Interrupts
  - Global and Individual Interrupt Masking

**N PACKAGE**
**(TOP VIEW)**




**FN PACKAGE†**
**(TOP VIEW)**




†Available third quarter 1986

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- **Additional Member of TMS7000 Family**
  - **Register-to-Register Architecture**
  - **Instructions Set Compatible with All TMS7000 Family Members**
  - **Eight Powerful Addressing Formats Including:**
    **Register-to-Register Arithmetic**
    **Indirect Addressing**
    **Indexed and Indirect Branches and Calls**
- **Development Support**
  - **Piggyback Prototyping Device, SE70CP162**
  - **Low Cost Evaluation Module**
  - **Full Feature Development System**
  - **Assembler/Linker Cross Support for Popular Hosts**

## description

The TMS70C42 is an 8-bit CMOS microcomputer that contains 4K bytes of on-chip ROM, 256 bytes of on-chip RAM, a flexible serial port, three timers, and 32 I/O lines. The TMS70C42 features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring the use of an accumulator (e.g., ADD, R24, R245; add register 24 to register 245 and store the result in register 245).

The TMS70C02 is the microprocessor version of the TMS70C42, having no on-chip ROM. The TMS70C02 uses 20 of the I/O lines for address, data, and bus control. The TMS70C02 can be used in large ROM applications and typical microcomputer applications that take advantage of on-chip features such as the UART, RAM, and timers.

Unless otherwise noted, the use of the term TMS70C42 in this document refers to both the TMS70C42 and TMS70C02.

The TMS70C42 is a low-cost microcomputer that is ideal for low power or battery powered operations. The high noise immunity, wide operation conditions and ranges of CMOS, and high performance CPU and internal peripherals allow flexible system designs in industrial, automotive, computer, and telecom applications.

The 16-bit timers, with their associated 16-bit capture latch and timer outputs, simplify A/D conversions, pulse width measurements, and other time-critical application designs.

The unique serial port has many powerful features allowing operation in various selectable protocols. It also supports direct networking for processor-to-processor communications.

When power consumption is critical, the TMS70C42 can idle selectable sections of the microcomputer (e.g., Timer 1, Timer 2, or UART) and use power only where needed. Also, the entire processor can be halted while retaining the 256 bytes of internal RAM over a wide range of supply voltages.

The TMS70C42 instruction set is compatible with that of all TMS7000 family members, allowing easy transition between members.



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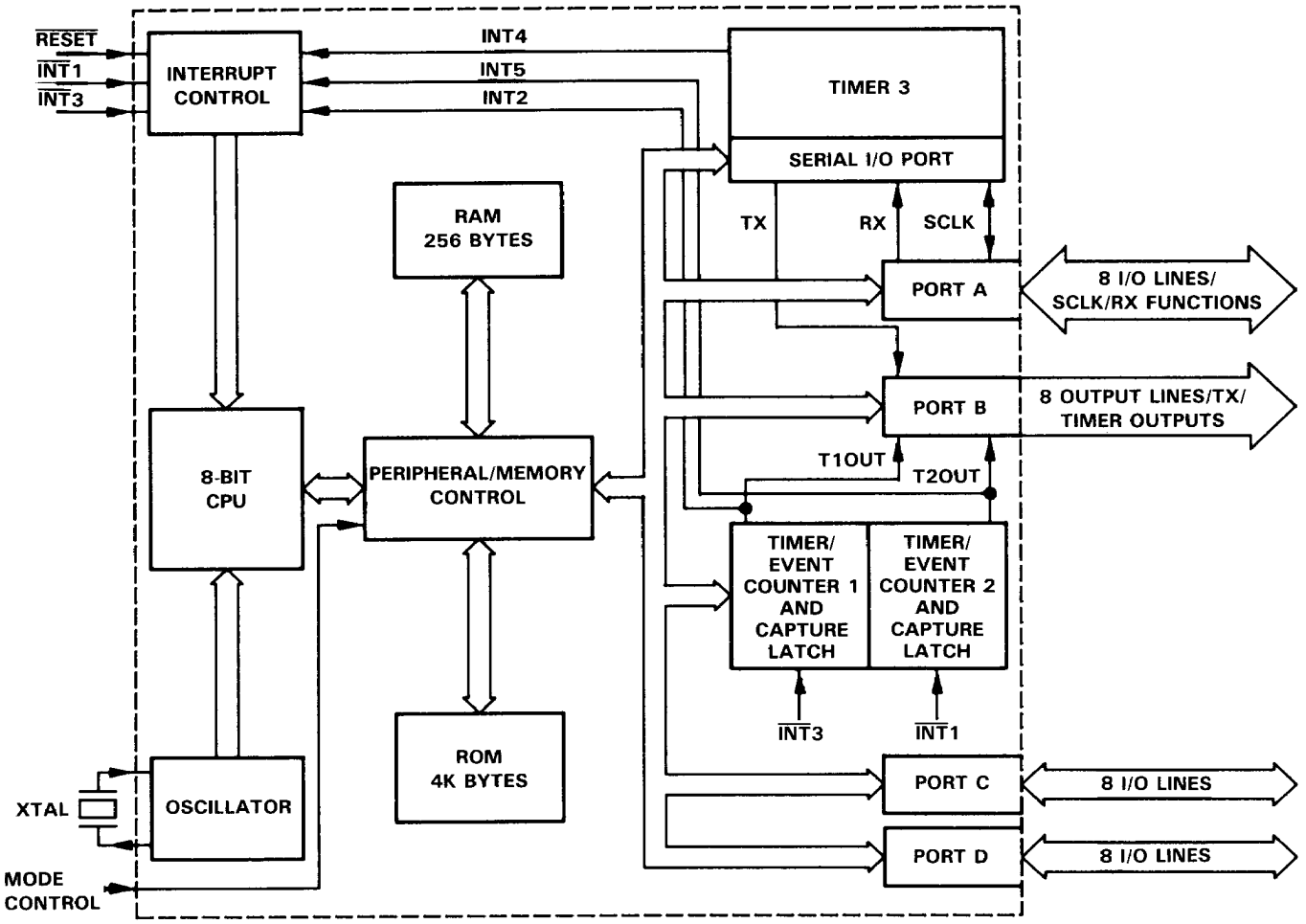
## functional block diagram



## pin descriptions

| NAME | PIN NUMBER | | I/O | DESCRIPTION |
|---|---|---|---|---|
| | N PACKAGE | FN PACKAGE | | |
| A0(LSB) | 6 | 7 | I/O | Port A is a bidirectional data port. |
| A1 | 7 | 8 | I/O | |
| A2 | 8 | 9 | I/O | |
| A3 | 9 | 10 | I/O | |
| A4/SCLK | 10 | 11 | I/O | Data I/O/Serial port clock |
| A5/RXD | 16 | 18 | I/O | Data I/O/Serial port input |
| A6/EC2 | 15 | 16 | I/O | Data I/O/Timer 2 event counter |
| A7/EC1 | 11 | 12 | I/O | Data I/O/Timer 1 event counter |
| B0/T2OUT | 3 | 3 | O | Data output/Timer 2 underflow toggles output |
| B1/T1OUT | 4 | 4 | O | Data output/Timer 1 underflow toggles output |
| B2 | 5 | 5 | O | Data output |
| B3/TXD | 37 | 41 | O | Data output/Serial port output |
| B4/ALATCH | 38 | 42 | O | Data output/Memory interface address latch strobe |
| B5/R/$\overline{W}$ | 1 | 1 | O | Data output/Memory interface Read/Write signal |
| B6/$\overline{ENABLE}$ | 39 | 43 | O | Data output/Memory interface enable strobe |
| B7/CLKOUT | 2 | 2 | O | Data output/Memory interface clock |
| C0 | 28 | 31 | I/O | Port C is a bidirectional data port. In Peripheral Expansion, Full Expansion, and Microprocessor modes, Port C is a multiplexed low address and data bus. |
| C1 | 29 | 32 | I/O | |
| C2 | 30 | 33 | I/O | |
| C3 | 31 | 34 | I/O | |
| C4 | 32 | 35 | I/O | |
| C5 | 33 | 36 | I/O | |
| C6 | 34 | 37 | I/O | |
| C7 | 35 | 38 | I/O | |
| D0 | 27 | 30 | I/O | Port D is a bidirectional data port. In Full Expansion and Microprocessor modes, Port D is the high address bus. |
| D1 | 26 | 29 | I/O | |
| D2 | 24 | 27 | I/O | |
| D3 | 23 | 26 | I/O | |
| D4 | 22 | 25 | I/O | |
| D5 | 21 | 24 | I/O | |
| D6 | 20 | 22 | I/O | |
| D7 | 19 | 21 | I/O | |
| $\overline{INT1}$ | 13 | 14 | I | Highest priority maskable, software programmable interrupt |
| $\overline{INT3}$ | 12 | 13 | I | Lower priority maskable, software programmable interrupt |
| $\overline{RESET}$ | 14 | 15 | I | Device reset |
| MC | 36 | 40 | I | Mode control pin |
| XTAL2/CLKIN | 17 | 19 | I | Crystal input for control of internal oscillator |
| XTAL1 | 18 | 20 | O | Crystal output for control of internal oscillator |
| $V_{CC}$ | 25 | 28 | | Supply voltage (2.5 V-6.0 V) |
| $V_{SS}$ | 40 | 23,39,44 | | Ground reference |



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## architecture

### memory modes

The TMS70C42 can be configured to reference up to 64K bytes of ROM and RAM and has four different operating modes allowing the optimization of the on-chip versus off-chip memory for each application. These modes are Single-Chip, Peripheral Expansion, Full Expansion, and Microprocessor modes. The table below shows the number of I/O pins and the amount of external address space available in each of the different modes. Note that the TMS70C02 normally operates in the Microprocessor mode only.

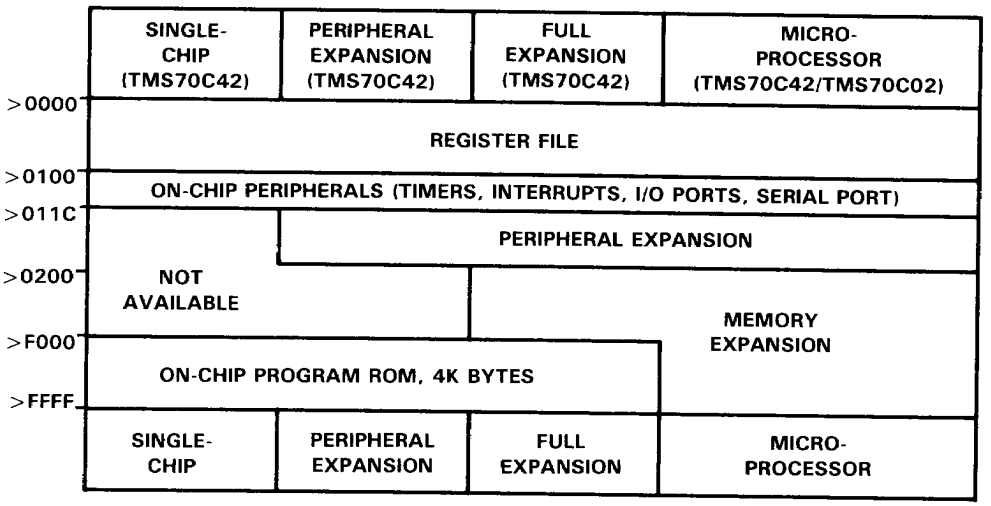
| | SINGLE-CHIP | PERIPHERAL EXPANSION | FULL EXPANSION | MICRO-PROCESSOR |
|---|---|---|---|---|
| DEVICE | TMS70C42 | TMS70C42 | TMS70C42 | TMS70C42/TMS70C02 |
| I/O Pins: | | | | |
| Bidirectional | 24 | 16 | 8 | 8 |
| Output only | 8 | 4 | 4 | 4 |
| Expansion Bus: | | | | |
| Multiplexed Address/Data lines | 0/0 | 8/8 | 16/8 | 16/8 |
| Control lines | 0 | 4 | 4 | 4 |
| Memory Space: | | | | |
| RAM | 256 | 256 | 256 | 256 |
| ROM† | 4096 | 4096 | 4096 | 0 |
| Internal Peripheral File | 28 | 25 | 23 | 23 |
| External Peripheral File | 0 | 231 | 233 | 233 |
| External Memory | 0 | 0 | 60928 | 65024 |

†The first six bytes of ROM (>F000->F005) are reserved.

| MODE | MODE SELECT CONDITIONS | | |
|---|---|---|---|
| | MC PIN | I/O CONTROL 0 (P0) BIT7 | BIT6 |
| Single-Chip | 0 V | 0 | 0 |
| Peripheral Expansion | 0 V | 0 | 1 |
| Full Expansion | 0 V | 1 | 0 |
| Microprocessor | $V_{CC}$ | X | X |

X = Don't Care.

memory map



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### peripheral memory map

| REGISTER | ADDRESS | NAME | NOTE | FUNCTION |
|---|---|---|---|---|
| P0 | >0100 | IOCNT0 | 3 | Interrupts 1, 2, and 3, expansion mode control |
| P1 | >0101 | IOCNT2 | | Polarity and edge/level control for $\overline{INT1}$ and $\overline{INT3}$ |
| P2 | >0102 | IOCNT1 | 3 | Interrupts 4 and 5 |
| P3 | >0103 | | | Reserved |
| P4 | >0104 | APORT | | A port data value |
| P5 | >0105 | ADDR | | A port direction register |
| P6 | >0106 | BPORT | 1 | B port data value |
| P7 | >0107 | | | Reserved |
| P8 | >0108 | CPORT | 1 | C port data value |
| P9 | >0109 | CDDR | 1 | C port direction register |
| P10 | >010A | DPORT | 2 | D port data value |
| P11 | >010B | DDDR | 2 | D port direction register |
| P12 | >010C | T1MSDATA | 3 | Timer 1 MSB reload register/MSB readout latch |
| P13 | >010D | T1LSDATA | 3 | Timer 1 LSB reload register/LSB decrementer value |
| P14 | >010E | T1CTL1 | 3 | Timer 1 control register 1/MSB readout latch |
| P15 | >010F | T1CTL0 | 3 | Timer 1 control register 0/LSB capture latch value |
| P16 | >0110 | T2MSDATA | 3 | Timer 2 MSB reload register/MSB readout latch |
| P17 | >0111 | T2LSDATA | 3 | Timer 2 LSB reload register/LSB decrementer value |
| P18 | >0112 | T2CTL1 | 3 | Timer 2 control register 1/MSB readout latch |
| P19 | >0113 | T2CTL0 | 3 | Timer 2 control register 0/LSB capture latch value |
| P20 | >0114 | SMODE | | Serial port mode control register |
| P21 | >0115 | SCTL0 | | Serial port control register 0 |
| P22 | >0116 | SSTAT | | Serial port status register |
| P23 | >0117 | T3DATA | 3 | Timer 3 reload register/decrementer value |
| P24 | >0118 | SCTL1 | | Serial port control register 1 |
| P25 | >0119 | RXBUF | | Receiver buffer |
| P26 | >011A | TXBUF | | Transmitter buffer |
| P27 | >011B | | | Reserved |
| P28-P255 | >011C->011F | | | Peripheral expansion |

NOTES: 1. P8, P9, and the most significant nibble of P6 become off-chip in Peripheral Expansion, Full Expansion, and Microprocessor modes.
2. P10 and P11 become off-chip in Full Expansion and Microprocessor modes. All other addresses between P0 and P27 inclusive remain on-chip in all expansion modes.
3. Exercise caution when using logical instructions (e.g., ANDP, ORP, XORP) on these registers because of the different read/write functions.

### interrupt priorities

The TMS70C42 has five interrupt levels plus $\overline{RESET}$. These levels are defined as follows:

Level 0: $\overline{RESET}$ (highest priority)
Level 1 ($\overline{INT1}$): External, user-defined, software programmable control over edge/level triggering and polarity
Level 2 (INT2): Timer 1
Level 3 ($\overline{INT3}$): External, user-defined, software programmable control over edge/level triggering and polarity
Level 4 (INT4): Serial port TX ready, RX full, or Timer 3
Level 5 (INT5): Timer 2

### device initialization

Interrupt level 0 ($\overline{\text{RESET}}$) cannot be masked and will be recognized immediately, even in the middle of an instruction. To execute the level 0 interrupt, the $\overline{\text{RESET}}$ pin must be held low for a minimum of 1.25 internal clock cycles ($t_{c(C)}$) to guarantee recognition by the device. During assertion of the $\overline{\text{RESET}}$ pin, the following conditions for the indicated locations occur.

| PF LOCATIONS | LOCATION | RESET RESULT |
|---|---|---|
| P5, P9, P11 | Data Direction Registers | Set to all 0s |
| P4, P8, P10 | Port A, C, D Output Data Flip Flops | Not affected |
| P6 | Port B Output Data Flip Flops | Set to all 1s |
| P0, P1 | IOCNT0, IOCNT2 | Set to all 0s<br>NOTE: INT1FLG-INT3FLG are cleared |
| P2 | IOCNT1 | Bits 3, 2, 0 set to 0<br>Bits 7, 6, 5, 4, 1 not affected<br>NOTE: INT4FLG is not cleared<br>NOTE: INT5FLG is cleared |
| P21 | SCTL0 | Bits 7, 2, 1, 0 set to 0<br>Bit 6 set to 1<br>Bits 5, 4, 3 not affected |
| P22 | SSTAT | Bits 6, 1 set to 0<br>Bits 2, 0 set to 1<br>Bits 7, 5, 4, 3 not affected |
| P24 | SCTL1 | Bits 6, 5, 4, 3, 2 set to 0<br>Bits 7, 1, 0 not affected |
| P14 | T1CTL1 | Bit 6 set to 0<br>All others not affected |
| P18 | T2CTL1 | Bits 7, 6 set to 0<br>All others not affected |

| CPU REGISTERS | RESET RESULT |
|---|---|
| Status Register | Cleared |
| Stack Pointer | Loaded with >01 |
| Program Counter | Old MSB, LSB loaded into Registers A and B<br>PC loaded with reset vector |

### I/O control registers

The I/O control registers are located in the Peripheral File and are responsible for memory mode definition and interrupt control. In the following figures, each bit in the I/O control registers is defined.

The INTn FLAG values are independent of the INTn ENABLE values. Writing a "1" to the INTn ENABLE will not clear the INTn FLAG. Writing a "1" to the INTn CLEAR bit will clear the corresponding INTn FLAG, but writing a "0" to the INTn CLEAR bit has no effect on the bit.



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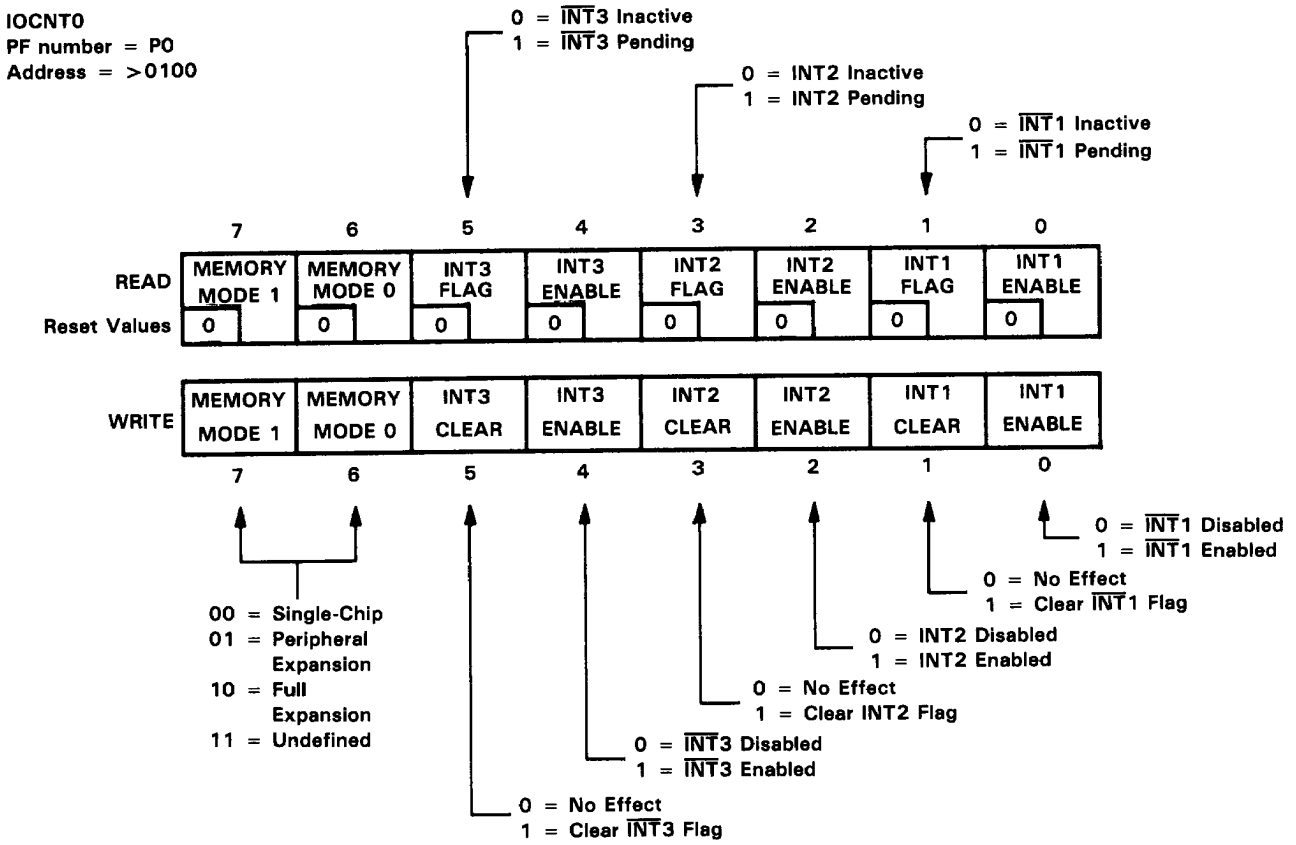



FIGURE 1. I/O CONTROL REGISTER 0 (IOCNT0)

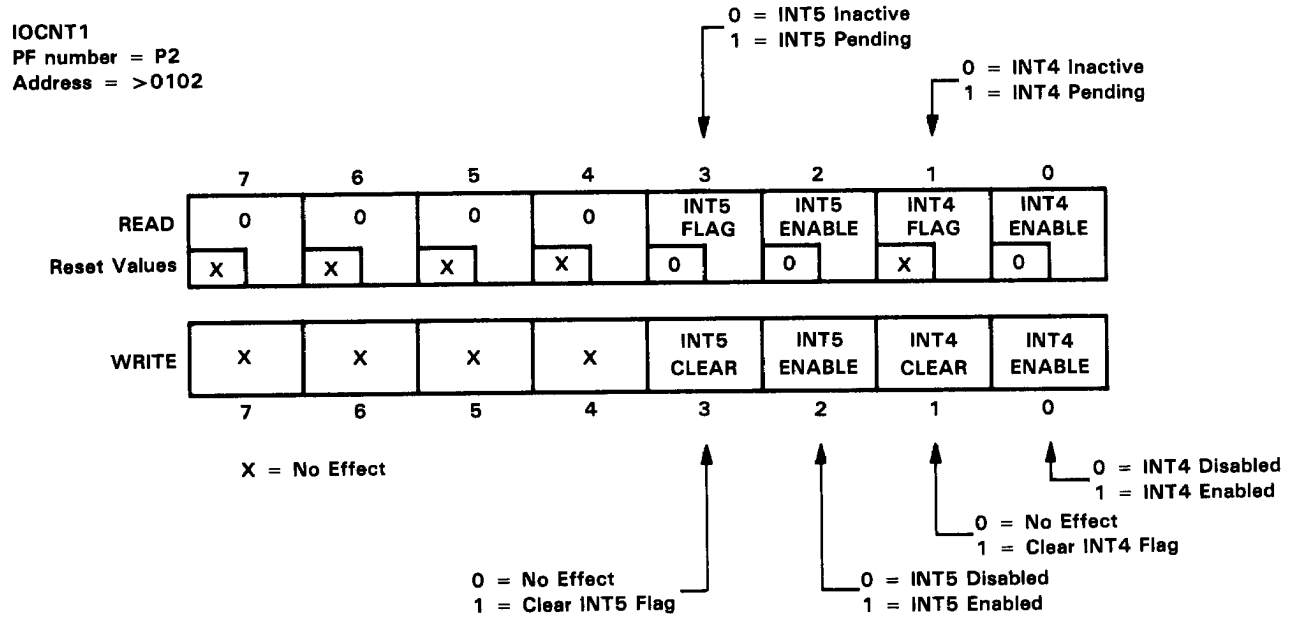
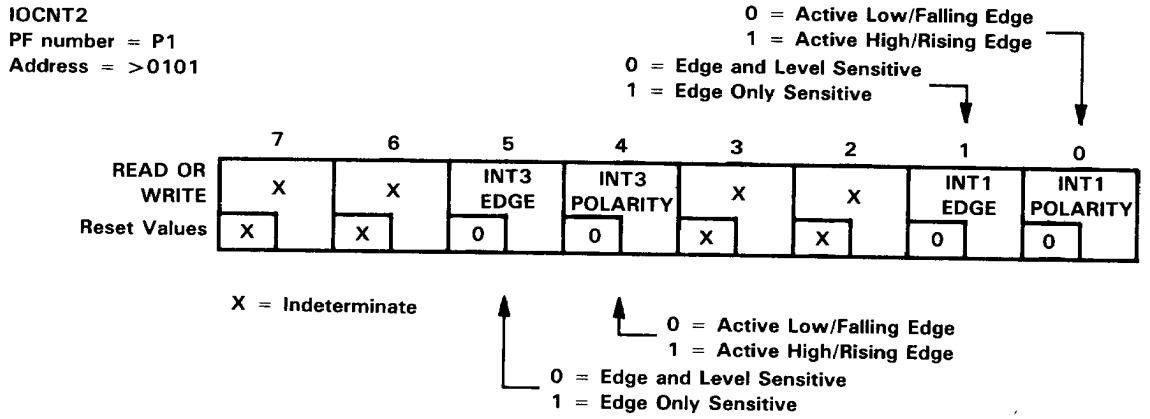



FIGURE 2. I/O CONTROL REGISTER 1 (IOCNT1)




NOTE 4: When changing the sense of $\overline{INT}1$ or $\overline{INT}3$, the interrupt will become active (set the FLAG bit and interrupt the CPU if enabled) if the level present at the interrupt pin corresponds with the new sense selected. Also, the corresponding capture latch will be loaded.

**FIGURE 3. I/O CONTROL REGISTER 2 (IOCNT2)**

**programmable timer/event counter**

The TMS70C42 features three on-chip timers with individual start/stop control bits. Timer 1 (shown in Figure 4) and Timer 2 consist of a 16-bit readable decrementer with a 16-bit reload register, a 16-bit capture latch, and a 5-bit non-readable prescaler with a 5-bit reload register. Timer 3 consists of an 8-bit readable decrementer with an 8-bit reload register and a 2-bit non-readable prescaler with a 2-bit reload register. Timer 3 can be used as a general-purpose timer or as a baud rate generator for the serial port.

**most significant byte readout latch**

This latch is shared between the most significant byte (MSB) of the decrementer and the MSB of the capture latch. It allows the complete 16-bit value of the decrementer or the capture latch to be sampled at one moment. The least significant byte (LSB) must be read first, which causes the MSB to be simultaneously loaded into the readout latch.

There is only one readout latch for each timer, but the same latch can be read from two addresses for easier programming (see the diagrams for Timer 1 and Timer 2).

Timer 1 MSB readout latch can be read from both P12 (>010C) and P14 (>010E). Similarly, Timer 2 MSB readout latch can be read from both P16 (>0110) and P18 (>0112).

Reading the LSB of the decrementer or capture latch will always update the contents of the readout latch. In order to correctly read the entire 16-bit value of the decrementer or capture latch, the LSB must be read first, which will load the MSB readout latch. The MSB readout latch must be read and stored before reading the LSB of either the decrementer or capture latch.

The order of 16-bit read operations should be:

Timer 1:
Decrementer: P13 then P12, or P13 then P14
Capture latch: P15 then P12, or P15 then P14

Timer 2:
Decrementer: P17 then P16, or P17 then P18
Capture latch: P19 then P16, or P19 then P18



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### timer 1 schematic diagram

A schematic diagram of Timer 1 is shown below. For clarity the details of the clock source selection and the power reduction mechanism are covered in Figure 6, Timer 1 Control Register.

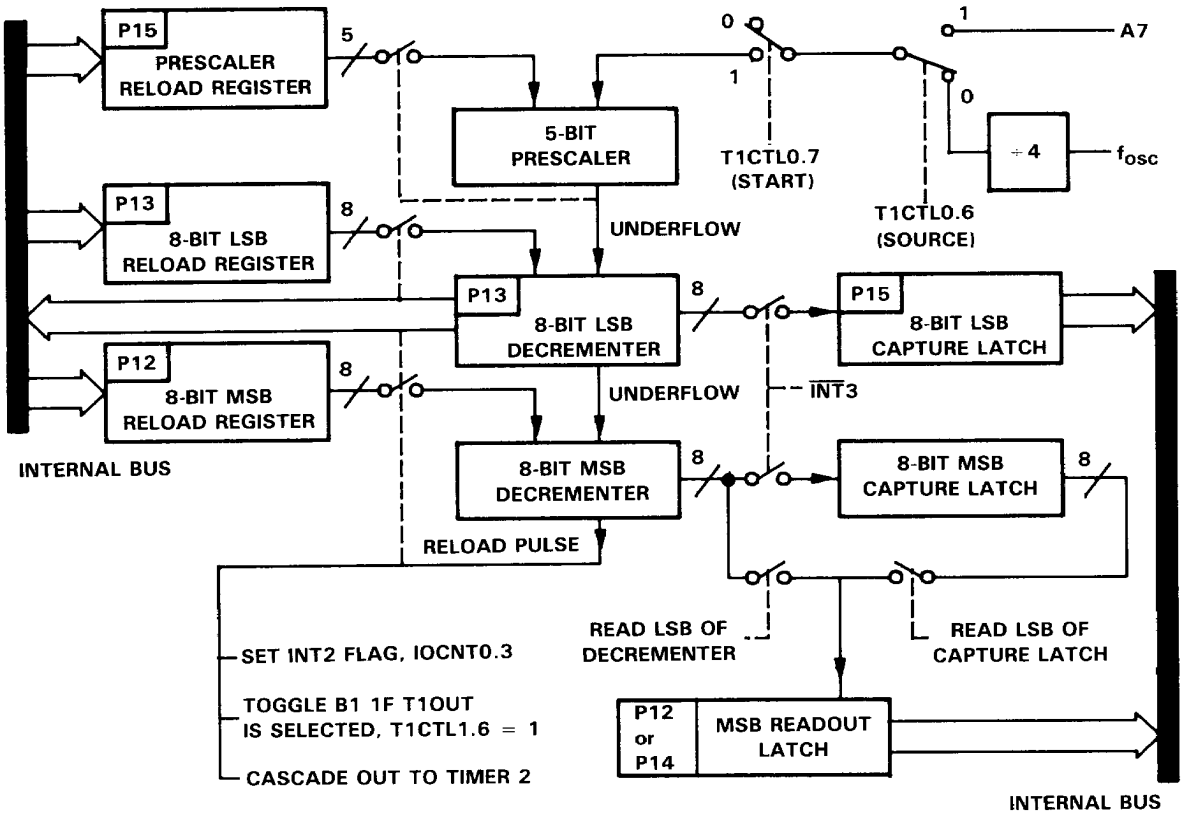


FIGURE 4. TIMER 1 SCHEMATIC DIAGRAM

timer 1 control registers

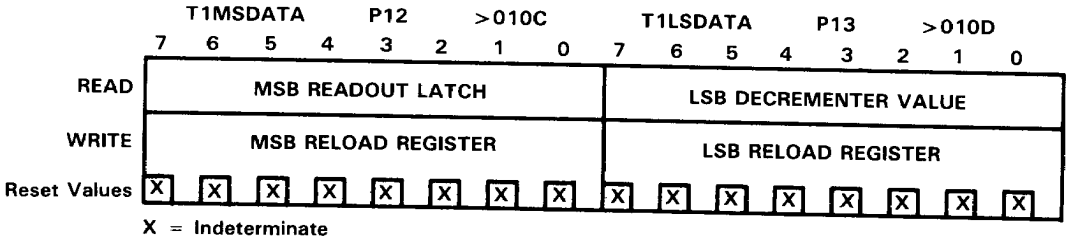


FIGURE 5. TIMER 1 DATA REGISTERS

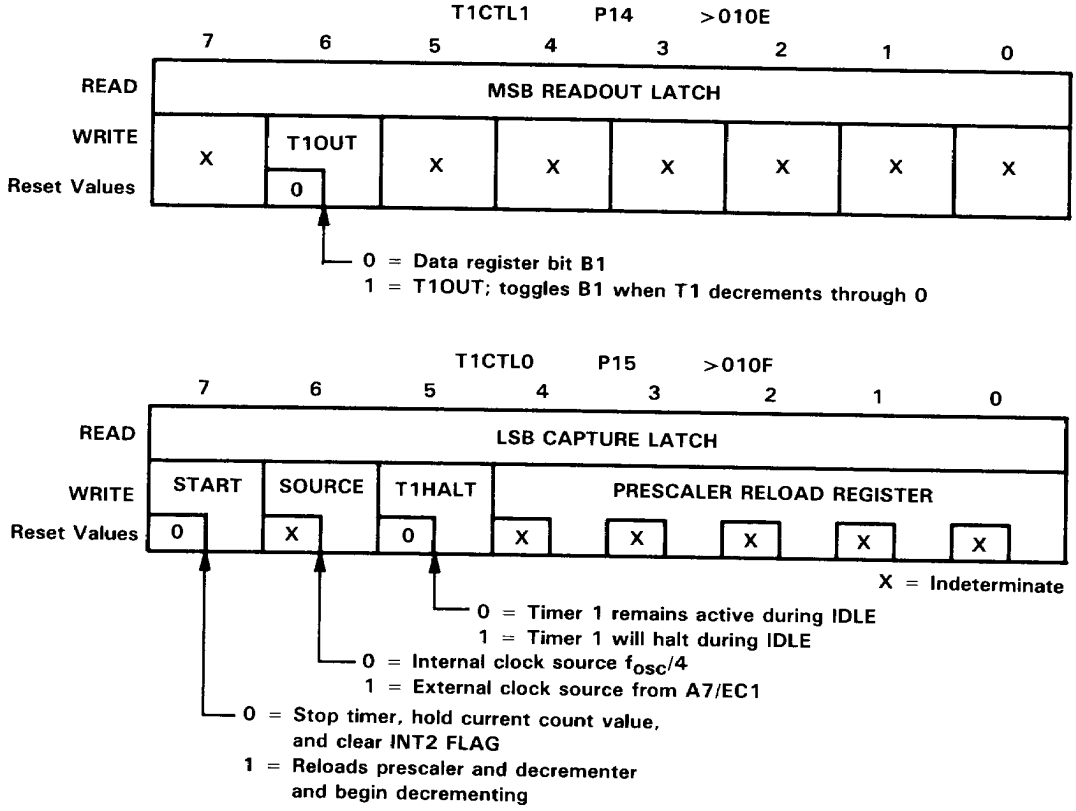


FIGURE 6. TIMER 1 CONTROL REGISTERS



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### timer 2 schematic diagram

A schematic diagram of Timer 2 is shown below. For clarity the details of the clock source selection and the power reduction mechanism are covered in Figure 9, Timer 2 Control Registers.

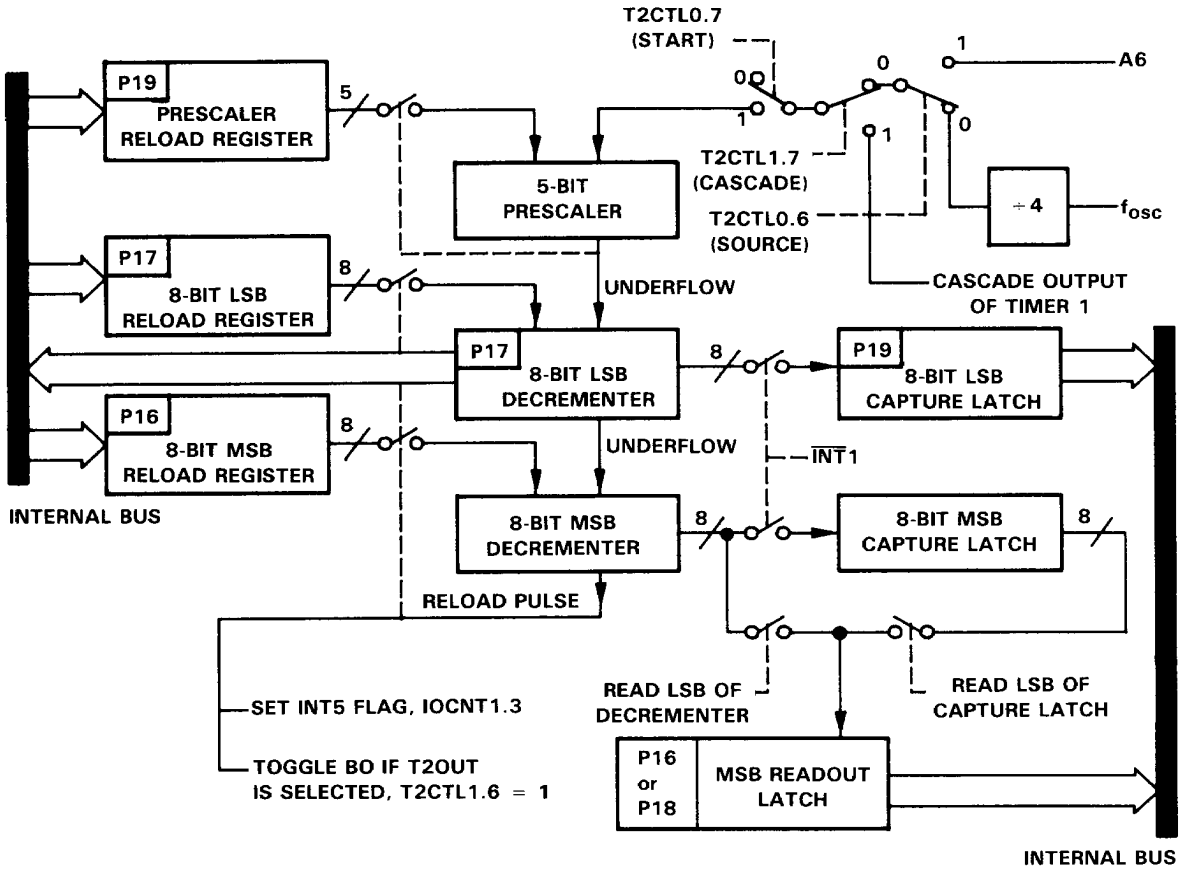



**FIGURE 7. TIMER 2 SCHEMATIC DIAGRAM**

timer 2 control registers

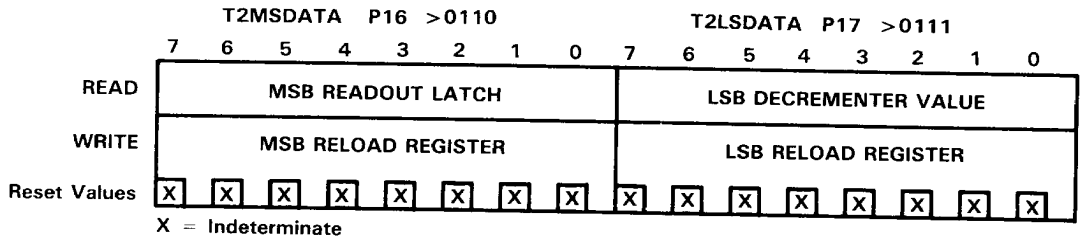
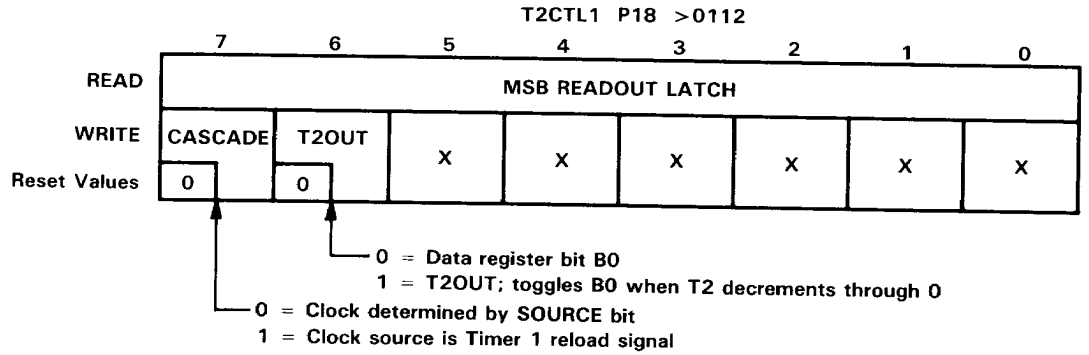



FIGURE 8. TIMER 2 DATA REGISTERS



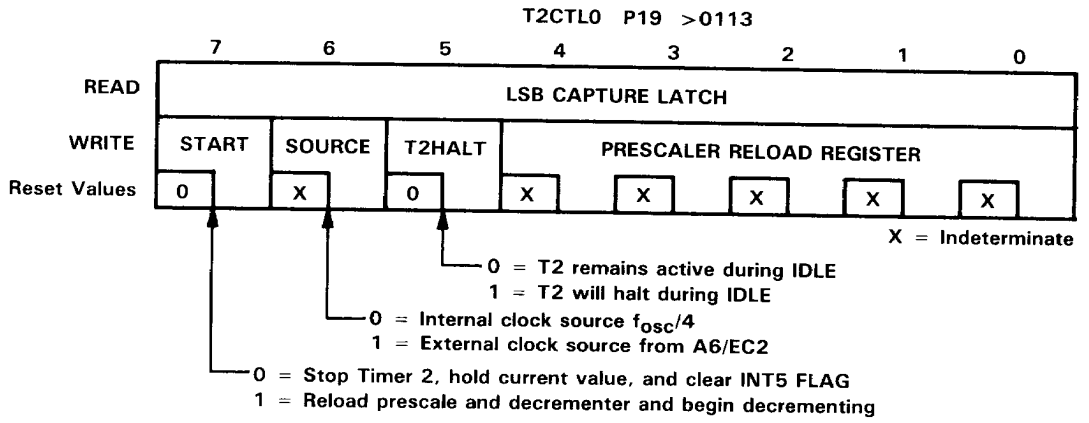




FIGURE 9. TIMER 2 CONTROL REGISTERS



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### timer 1 and timer 2 clock sources

**TIMER 1 CLOCK SOURCES**

| T1CTL0 BIT 6 (SOURCE) | CLOCK SOURCE | MODE |
|---|---|---|
| 0 | $f_{osc}/4$ | RTC (Real Time Clock) |
| 1 | A7, External | EC (Event Counter) |

**TIMER 2 CLOCK SOURCES**

| T2CTL0 BIT 6 (SOURCE) | T2CTL1 BIT 7 (CASCADE) | CLOCK SOURCE | MODE |
|---|---|---|---|
| 0 | 0 | $f_{osc}/4$ | RTC |
| 1 | 0 | A6, External | EC |
| X | 1 | Reload Signal of Timer 1 | CASCADE |

Bit 7 of timer control registers T1CTL0 and T2CTL0 is the START bit for Timer 1 and Timer 2, respectively. When a 0 is written to the START bit, the timer chain is disabled and frozen at the current count value, and Timer 1's INT2 FLAG or Timer 2's INT5 FLAG is set to 0. This differs from the TMS7042 since the interrupt flags will not be cleared when the timer is disabled. When a 1 is written to the START bit, regardless of whether it was a 0 or a 1 before, the prescaler and counter decrementers are loaded with the corresponding latch values, and the Timer/Event Counter operation begins.

When the prescaler and counter decrement through zero together, an interrupt flag is set and the prescaler and counter decrementers are immediately and automatically reloaded with the corresponding values from the reload registers and counting continues. The interrupts generated by the timers are INT2 for Timer 1 and INT5 for Timer 2.

Timers 1 and 2 each have a 16-bit capture latch which "captures" the current value of the counter whenever the appropriate input capture signal is generated. The capture latch values for Timer 1 and Timer 2 are loaded on the active edges of $\overline{INT3}$ and $\overline{INT1}$, respectively, whether or not the interrupts are enabled. Both capture latches are disabled during the IDLE instruction when their corresponding timer HALT bits are 1.

#### event counter (EC)

When Timer 1 or Timer 2 is in the EC mode, pins A7 and A6 are the decrementer clock sources for Timer 1 and Timer 2, respectively. The maximum clock frequency on A7 or A6 in the EC mode must not be greater than $f_{osc}/4$. The minimum pulse width must not be less than 1.25 machine cycles ($t_{C(C)}$). Each positive pulse transition decrements the count chain.

### timer output function

A timer output function exists on both Timer 1 and Timer 2 that allows the B1 and B0 outputs, respectively, to be toggled every time the timer decrements through zero. This function is enabled by the T1OUT bit and T2OUT bit (bit 6) in timer control registers T1CTL1 and T2CTL1.

When operating in the timer output mode, the B0 and/or B1 output can not be changed by writing to the B port data register. Writing to the respective timer's START bit will reload and start the timer, but will not toggle the output. The output will toggle only when the timer decrements through zero. The timer output feature is independent of INT2 and INT5 and, therefore, will operate with INT2 and INT5 enabled or disabled. Also, if the timer is active during the IDLE instruction, the timer output feature will continue to operate.

Whenever the T2OUT or T1OUT bit is returned to 0, B0 or B1 will become an output-only pin, like B2. The value in the B0 or B1 data register will be the last value output by the timer output function, so that B0 or B1 will not change as the T2OUT or T1OUT bit is returned to 0.

Whenever a read of the B port is performed, the value on the B0 pin will always be returned, so the current timer output value can be read by reading the B port.

The T1OUT and T2OUT bits are set to 0 by $\overline{\text{RESET}}$, so the timer output function will not be enabled unless the user sets the T1OUT or T2OUT bit to 1.

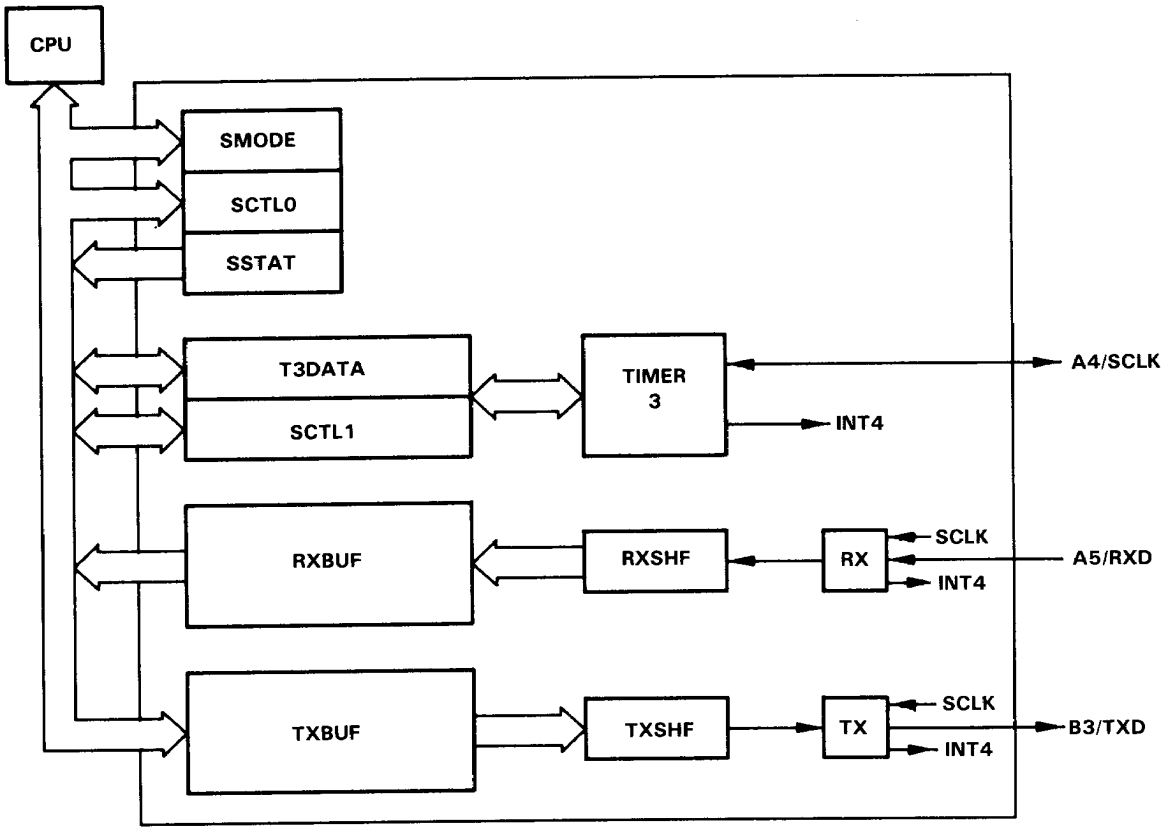
The Timer 2 output (T2OUT) cannot be used if Timer 1 and Timer 2 are cascaded together (CASCADE bit of T2CTL1 set to 1).

### serial port

The TMS70C42 contains a serial port which greatly enhances its I/O and communication capability. The serial port can operate in several modes which permit the TMS70C42 to interface with Universal Synchronous Asynchronous Receiver/Transmitter (USART) peripheral devices, as well as several microcomputers (e.g., TMS70C42, TMS7042, TMS7742, 6801, 8051). The serial port consists of a receiver (RX), transmitter (TX), and baud rate generator (Timer 3, T3). It is controlled and accessed through the following registers in the Peripheral File:

| REGISTER | ADDRESS | NAME | TYPE | FUNCTION |
|---|---|---|---|---|
| P20 | >0114 | SMODE | R/W | Serial Port Mode |
| P21 | >0115 | SCTL0 | R/W | Serial Port Control 0 |
| P22 | >0116 | SSTAT | READ | Serial Port Status |
| P23 | >0117 | T3DATA | R/W | Timer 3 Data |
| P24 | >0118 | SCTL1 | R/W | Serial Port Control 1 |
| P25 | >0119 | RXBUF | READ | Receiver Buffer |
| P26 | >011A | TXBUF | WRITE | Transmission Buffer |

For detailed register bit descriptions, refer to the *TMS7000 Family Data Manual,* part number SPND001.




NOTE 5. The INT4 sources are effectively wire-ORed together to generate only one INT4 input. The SCLK sources are wired together to generate only one SCLK input.

**FIGURE 10. SERIAL PORT FUNCTIONAL BLOCKS**

SMODE
PF number = P20
Address = >0114

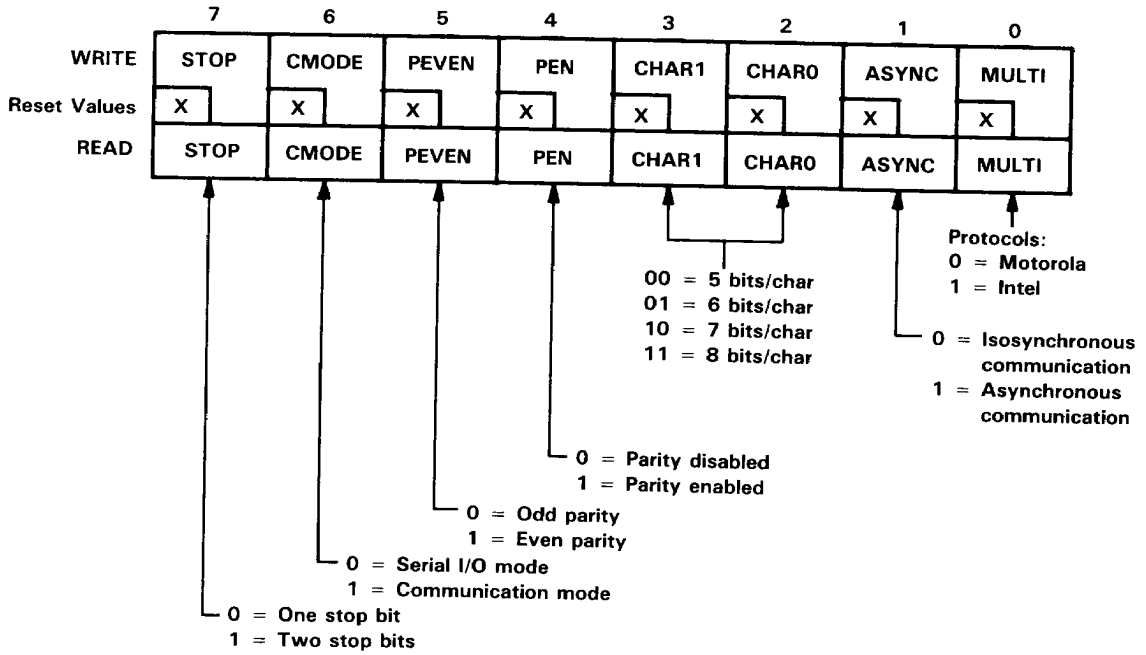



**FIGURE 11. SERIAL PORT MODE (SMODE)**

SMODE is the RX/TX control register that describes the character format and type of communication mode.



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SCTL0
PF number = P21
Address = > 0115

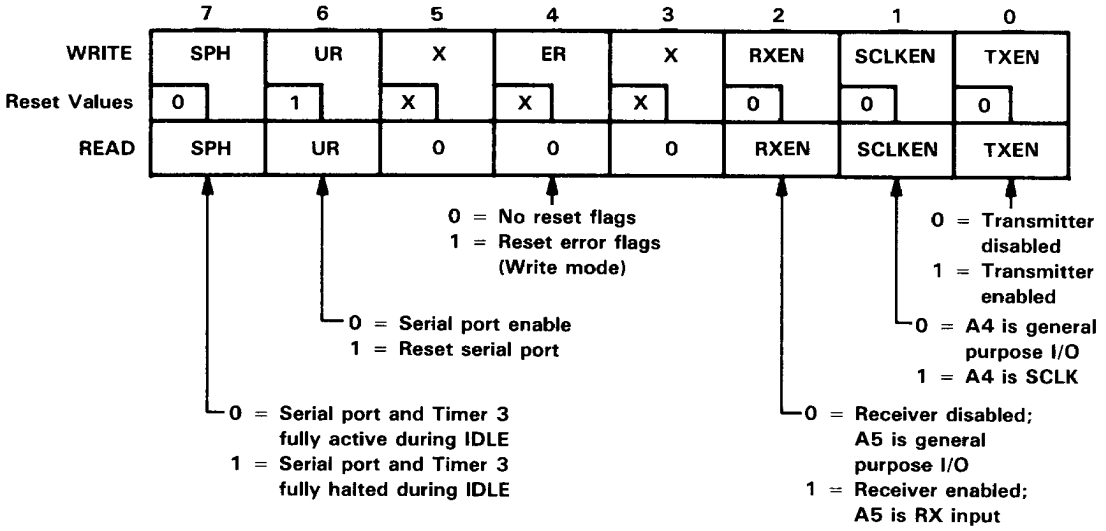


**FIGURE 12. SERIAL PORT CONTROL REGISTER 0 (SCTL0)**

SCTL0 is the RX/TX control register used to control the serial port functions such as TX and RX enable, clearing of error flags, and software enable.

SSTAT
PF number = P22
Address = >0116

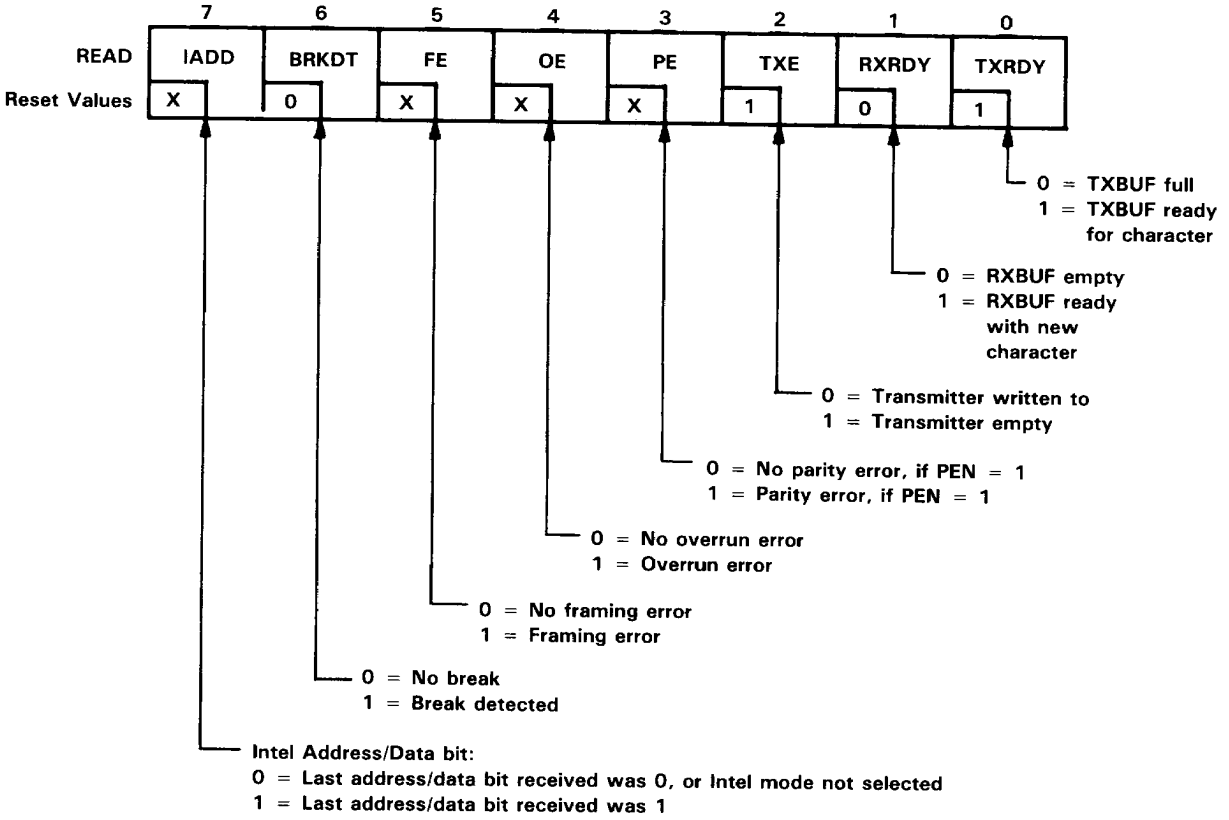


**FIGURE 13. SERIAL PORT STATUS (SSTAT)**

SSTAT is the read-only register used to report the status of the serial port. Bit 7 (IADD) stores the value of the last address/data bit received when using the Intel multiprocessor mode.

T3DATA
PF number = P23
Address = >0117


**FIGURE 14. TIMER 3 DATA REGISTER (T3DATA)**



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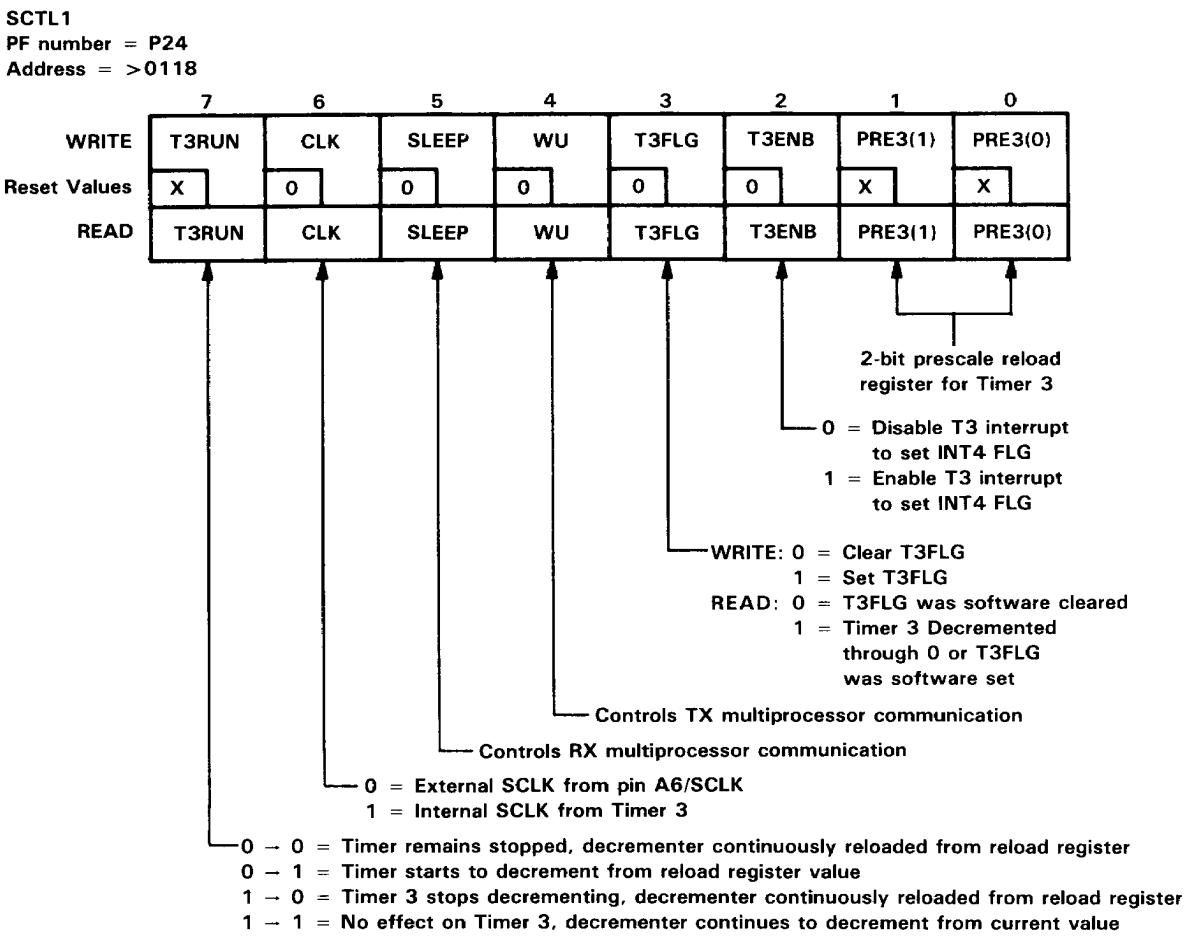


**FIGURE 15. SERIAL PORT CONTROL REGISTER (SCTL1)**

For a description of the individual timer bits in SCTL1, see the Timer 3 section of this document.

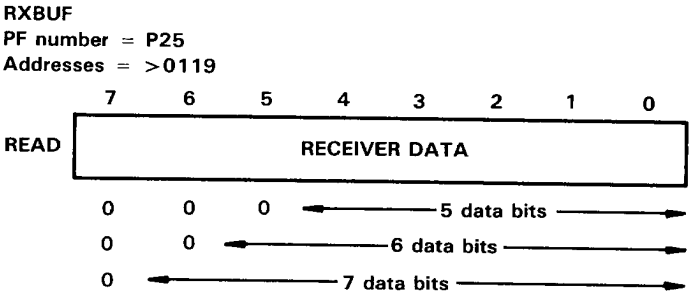


FIGURE 16. RECEIVER BUFFER (RXBUF)

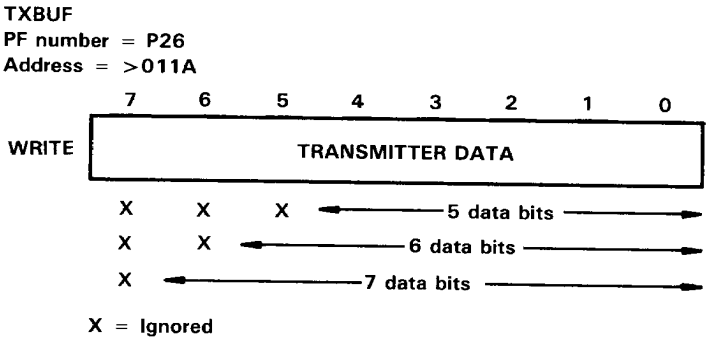


FIGURE 17. TRANSMITTER BUFFER (TXBUF)

**serial port clock sources**

The serial port can be clocked by Timer 3 or an external baud rate generator. The source of the serial clock (SCLK) is determined by the CLK bit (SCTL1 bit 6) and the SCLKEN bit (SCTL0 bit 1).

| SCKLEN | CLK | Serial Port Clock Operation |
|---|---|---|
| 1 | 1 | A4 is forced to output mode, independent of the data direction register (P5). Timer 3 provides the clock for the Serial Port which is output as SCLK on A4. |
| 1 | 0 | A4 is forced to input mode, independent of the data direction register (P5). An external signal applied to A4 provides the baud rate clock for the Serial Port. |
| 0 | 1 | A4 is available for general-purpose I/O. The clock for the serial port is provided by Timer 3 but is not output on any pin. |
| 0 | 0 | A4 is selected as general-purpose I/O with its direction register controlling the direction of A4. The serial port clock is taken from the A4 pin, so the clock can be provided by an external signal if the pin is in input mode (the same as the SCLKEN = 1, CLK = 0 option above), or by software if the pin is in output mode by writing to the A4 data register. |

If SCLKEN is changed from 1 to 0, A4 will have the direction selected by the A port direction register.

In any of these modes, reading from A4 will return the value present at the pin. SCLKEN and CLK are both set to 0 by $\overline{\text{RESET}}$. The A4 direction register is also set to 0 (input) by $\overline{\text{RESET}}$.



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**timer 3**

Timer 3 can be used as a general-purpose timer or as the clock generator for the serial port. Timer 3 is accessed through T3DATA and SCTL1. The Timer 3 clock source is an internal signal with the frequency equal to $f_{osc}/4$. Timer 3 consists of a 2-bit prescaler and an 8-bit counter. These are automatically preloaded from a 2-bit and an 8-bit reload register, respectively, whenever a register decrements through zero.

Timer 3 is continuously reloaded with the prescaler and decrementer reload register values while the START bit is 0. Timer 3 differs from Timer 1 and Timer 2 in that Timer 3 cannot be held at the value it contained when the START bit goes to 0. The timer begins decrementing when the START bit is changed from 0 to 1.

The Timer 3 START bit is not initialized by reset. If the Timer 3 START bit is 1 after reset, then Timer 3 will begin to decrement an indeterminate value. To prevent false starts, initalize the Timer 3 START bit to 0 after reset. The Timer 3 flag (SCTL1 bit 3) should also be set to 0 after reset.

Each time the timer decrements through zero, the Timer 3 flag is set to 1 and the INT4 FLAG is set to 1 if T3ENB (SCTL1 bit 2) is 1. Timer 3 and its flags are not affected by the serial port software reset (UR). Therefore, Timer 3 can be used independent of the serial port.

When using Timer 3 as the serial port clock source, the reload pulse (timer decremented through zero) output of Timer 3 goes to the serial port via a divide-by-two circuit, producing an equal mark-space ratio internal SCLK (see Timer 3 block diagram). The baud rate generated by Timer 3 is user-programmable and is determined by the value of the 2-bit prescaler and the 8-bit timer reload registers.

The equations for determining the output baud rates for both the asynchronous and isosynchronous modes are:

$$\text{Asynchronous Baud Rate} = \frac{f_{osc}}{64(PRR+1)(TRR+1)} = \frac{SCLK}{8}$$

$$\text{Isosynchronous Baud Rate} = \frac{f_{osc}}{8(PRR+1)(TRR+1)} = SCLK$$

where: $f_{osc}$ = frequency of the crystal or external system clock
TRR = Timer 3 decrementer reload register (P23)
PRR = Timer 3 prescale reload register (P24)
SCLK = Serial clock either input or output from the SCLK pin

The baud rate for the serial I/O mode is determined with the same equation used to determine the

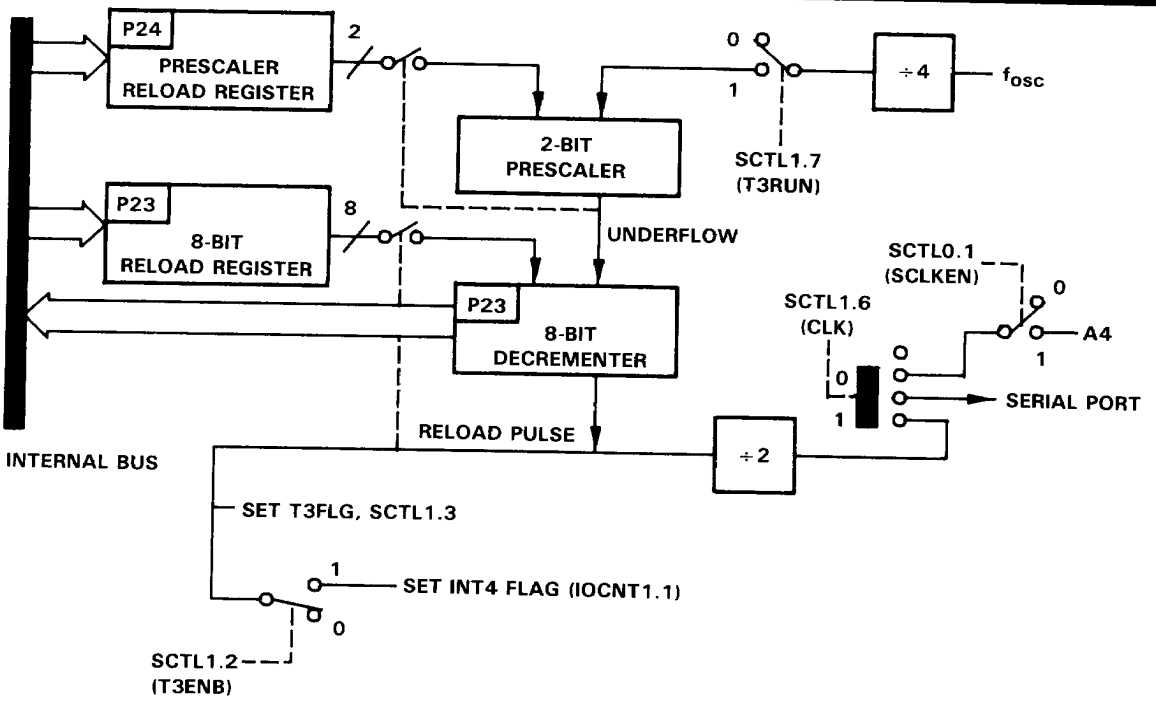


**FIGURE 18. TIMER 3 SCHEMATIC DIAGRAM**

**serial port initialization and reset**

After a system reset, the UR bit in SCTL0 will be set to 1 and the serial port will be held in its reset condition. The serial port registers are then set in the order shown below. A serial port reset can be performed by writing a 1 to the UR bit (SCTL0 bit 6) or by writing data to the SMODE register at any time. Whenever a write to the SMODE register is performed, the UR bit is set to 1 and the serial port will be reset. The data written to SMODE will become the new SMODE register contents.

Note that the Timer 3 START bit (bit 7) of SCTL1 is not initialized by reset.

**SERIAL PORT INITIALIZATION**

SET B3 DATA = 1
WRITE TO SMODE
WRITE TO SCTL0 (SET BIT 6 TO 0)
WRITE TO SCTL1

The BPORT pin 3 must be set to 1 to transmit. A BPORT read will directly read the values at the pins. Since most write operations execute a read modify write cycle, some instructions might disable the UART output pin (B3).

Avoid using ANDP and XORP instructions on Port B when the transmitter is operating. Use instructions such as MOVP, ORP, or STA to prevent setting B3 to 0. If an ORP instruction is used, make sure a 1 is ORed with B3.

A 0 must be written to the WU bit and the SLEEP bit when operating in the serial I/O mode.



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**UART reset by software**

Setting the UR bit (SCTL0 bit 6) to 1 affects the following:

| | |
|---|---|
| SCTL0 | Bits 7, 2, 1, 0 set to 0<br>Bit 6 set to 1<br>Bits 5, 4, 3 not affected |
| SSTAT | Bits 6, 1 set to 0<br>Bits 2, 0 set to 1<br>Bits 7, 5, 4, 3 not affected |
| SCTL1 | Bits 6, 5, 4 set to 0<br>Bits 7, 3, 2, 1, 0 not affected |
| Pin 36 (B3/TXD) | Outputs the value of bit 3 of P6 |
| Pin 10 (A4/SCLK) | Configures to the corresponding values stored in P4 and P5 |
| Pin 16 (A5/RXD) | Configures to the corresponding values stored in P4 and P5 |

You cannot write to the affected bits of SCTL0 and SCTL1 while the UR bit is set to 1. The configuration of all bits in SCTL0 can be written to with a single instruction as long as the value of bit 6 (UR) within that instruction is 0.

**software example**

The following software example initializes the TMS70C42.

```
*************************************************************
*    R E S E T    A N D     I N I T I A L I Z A T I O N    *
*************************************************************
*
*         E Q U A T E   T A B L E
*
APORT   EQU   P4          Aport Data Register
BPORT   EQU   P6          Bport Data Register
CPORT   EQU   P8          Cport Data Register
DPORT   EQU   P10         Dport Data Register
ADDR    EQU   P5          Aport Data Direction Register
CDDR    EQU   P9          Cport Data Direction Register
DDDR    EQU   P11         Dport Data Direction Register
*
*         I/O Control Registers
*
IOCNT0 EQU    P0          Interrupts 1,2,3 & Expansion Mode
IOCNT1 EQU    P2          Interrrupts 4, and 5
IOCNT2 EQU    P1          Int 1 & 3  Polarity and Level Control
*
*         Timer 1 Registers
*
T1CTL0 EQU    P15         Timer 1 Control Register 0
T1CTL1 EQU    P14         Timer 1 Control Register 1
T1LSDA EQU    P13         Timer 1 LSB Reload Register
T1MSDA EQU    P12         Timer 1 MSB Reload Register
PRESC1 EQU    >03         Timer 1 Prescale value
T1MSB  EQU    >FF         Timer 1 MSB value
T1LSB  EQU    >00         Timer 1 LSB value
```

```
*
*         Timer 2 Register
*
T2CTL0 EQU   P19         Timer 2 Control Register 0
T2CTL1 EQU   P18         Timer 2 Control Register 1
T2LSDA EQU   P17         Timer 2 LSB Reload Register
T2LSDA EQU   P19         Timer 2 MSB Reload Register
PRESC2 EQU   >00         Timer 2 Prescale value
T2MSB  EQU   >08         Timer 2 MSB value
T2LSB  EQU   >0F         Timer 2 LSB value
*
*         Uart Registers
*
T3DATA EQU   P23         Timer 3 Reload Register
SMODE  EQU   P20         Serial Port Mode Control Register
SCTL0  EQU   P21         Serial Port Control Register 0
SCTL1  EQU   P24         Serial Port Control Register 1
*
*  T H I S   I S   T H E   R E S E T   E N T R Y   P O I N T
*  ------------------------------------------------------
*
START  DINT                        Disable Interrupts
*
       MOVP  %?01000000,SCTL1      HALT Timer 3, SLEEP & WU Bits OFF
*
       MOV   %100,B                Set Stack Pointer to R100
       LDSP                        Load Stack Pointer
*
*  I N T E R R U P T S
*  -------------------
       MOVP  %?00101110,IOCNT0  Set MODE, INTs 1,2,3, clear all flags
       MOVP  %?00001011,IOCNT1  Set INTs 4,5, clear all flags
       MOVP  %?00000000,IOCNT2  Set INTs sense, type (level/edge)
*
*  P O R T   D A T A
*  -----------------
       MOVP  %?00001000,APORT   Initialize PORT A
       MOVP  %?11111001,BPORT   Init PORT B (B3=1 for UART operation)
       MOVP  %?11111111,CPORT   Initialize PORT C
       MOVP  %?11001011,DPORT   Initialize PORT D
       MOVP  %?10001110,ADDR    Initialize PORT A  data direction
       MOVP  %?10111111,CDDR    Initialize PORT C  data direction
       MOVP  %?01001001,DDDR    Initialize PORT D  data direction
*
*  T I M E R S    TIMER 1
*  ----------------------
*  Timer 1 is an internal real time clock which interrupts
*  the CPU on interrupt level 2.
*
       MOVP  %?00000000,T1CTL1         Timer 1 output turned off
       MOVP  %T1LSB,T1LSDA             LSB Timer latch value for T1
       MOVP  %T1MSB,T1MSDA             MSB Timer latch value on 70C42
       MOVP  %?10000000,PRESC1 T1CTL0  Start 1/2
```

```
*
*  TIMER 2
*  -------
*  Timer 2 will output a square wave at the frequency determined
*  by the timer values loaded. The square wave will be output on
*  BPORT 0. Timer 2 will run continuously, without futher CPU
*  servicing.
*
       MOVP  %?01000000,T2CTL1          Enable Timer 2 output on B0,cascade off
       MOVP  %T2LSB,T2LSDA              LSB Timer latch value for T2
       MOVP  %T2MSB,T2LSDA              MSB  timer latch value on 70C42
       MOVP  %?10000000+PRESC2,T2CTL0   Start bit ON + Prescale value
*
*  TIMER 3
*  -------
       MOVP  %B300,T3DATA        300 BAUD RECEIVE/TRANSMITT
*
*  S E R I A L  P O R T
*  --------------------
       MOVP  %?01111110,SMODE    DA=8,ST=1,PA=EV,PRCL=MOTR
       MOVP  %?00010100,SCTL0    Reset error,EN RX, Disable SCLK & TD
       MOVP  %?11000001,SCTL1    START UART,CLK=INT,PS=1, SLEEP & WU=Off
*
*    E N D   O F   I N I T I A L I Z A T I O N
*
```

### power reduction mode

The TMS70C42 supports the Wake-up mode for low power consumption. The Wake-up mode is entered via execution of the IDLE instruction. The power reduction mechanisms for each timer and the UART are completely independent of each other and are selected individually via the T1HALT, T2HALT, and SPH bits, located in the T1CTL0, T2CTL0, and SCTL0 registers, respectively. The Wake-up mode is exited by assertion of an enabled interrupt to the CPU or $\overline{\text{RESET}}$.

The following table describes the exit from the power-reduction state. The exit options must be enabled in the appropriate control registers prior to executing the IDLE instruction and entering the Wake-up mode.

| MODE | FUNCTIONAL BLOCK STATUS | | | ENTER MODE VIA | EXIT† MODE VIA |
|---|---|---|---|---|---|
| | CPU | TI, T2, T3-UART | OSC. | | |
| Wake-up | Halted | Individually programmed as fully active or halted | Active | IDLE | $\overline{\text{RESET}}$<br>$\overline{\text{INT}}$1<br>INT2<br>$\overline{\text{INT}}$3<br>INT4<br>INT5 |

†Interrupts must be enabled to exit.

Since all synchronization is lost during an IDLE when SPH = 1, it is recommended that the serial port be completely reset after exiting IDLE.

### I/O port operation during power reduction

The following table indicates the state of the memory expansion ports (B, C, and D) in the low power mode, for each of the expansion modes. All of the other I/O pins will maintain their current direction (input or output) and will continue to output the same data if in output mode. No outputs become tri-state when Wake-up mode is entered.

| I/O PIN | SINGLE-CHIP | PERIPHERAL EXPANSION | FULL EXPANSION AND MICROPROCESSOR |
|---|---|---|---|
| CLOCKOUT (B7) | B7 data register value | 0 | 0 |
| $\overline{\text{ENABLE}}$ (B6) | B6 data register value | 1 | 1 |
| R/$\overline{\text{W}}$ (B5) | B5 data register value | 1 | 1 |
| ALATCH (B4) | B4 data register value | 0 | 0 |
| ADDR/DATA (C7-C0) | Individual I/O | X | X |
| HIGH ADDR (D7-D0) | Individual I/O | X | X |

X = Indeterminate

### capture latch operation during power reduction

In Wake-up mode, Timer 1's capture latch will not be loaded when the $\overline{\text{INT3}}$ pin is taken to its active level if T1HALT is 1. If T1HALT is 0 then the capture latch will be loaded every time the $\overline{\text{INT3}}$ pin is taken to its active level, regardless of the value of the INT3EN flag. Similarly, Timer 2's capture latch in Wake-up mode will not be loaded when the $\overline{\text{INT1}}$ pin is taken to its active level if T2HALT is 1. If T2HALT is 0, then the capture latch will be loaded every time the $\overline{\text{INT1}}$ pin is taken to its active level, regardless of the value of the INT1EN flag.

Once the TMS70C42 has been brought out of Wake-up mode, the capture latch will always be loaded when the appropriate interrupt pin is taken to its active level.



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## WIDE VOLTAGE CMOS SPECIFICATION

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 6) . . . . . −0.3 V to 7 V
Input voltage range . . . . . −0.3 V to $V_{CC}$ + 0.3 V
Output voltage range . . . . . −0.3 V to $V_{CC}$ + 0.3 V
Maximum I/O buffer current . . . . . ±10 mA
Maximum supply current, $I_{CC}$ . . . . . 60 mA
Maximum supply current, $I_{SS}$ . . . . . −60 mA
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values in this data sheet are with respect to $V_{SS}$.

### recommended operating conditions

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 2.5 | | 6.0 | V |
| $V_{IH}$ | High-level input voltage | All inputs except MC,XTAL2 | $V_{CC}$ = 3 V to 6 V | 0.70 $V_{CC}$ | | | V |
| | | | $V_{CC}$ = 2.5 V to 3 V | 0.75 $V_{CC}$ | | | V |
| | | MC, XTAL2 | $V_{CC}$ = 2.5 V to 6 V | 0.8 $V_{CC}$ | | | V |
| $V_{IL}$ | Low-level input voltage | All inputs except MC and XTAL2 | | | | 0.3 $V_{CC}$ | V |
| | | MC, XTAL2 | | | | 0.2 $V_{CC}$ | V |
| $T_A$ | Operating free-air temperature | Commercial (TMS70C42NL) | | 0 | | 70 | °C |
| | | Industrial (TMS70C42NA) | | −40 | | 85 | °C |

## electrical characteristics over full range of operating conditions

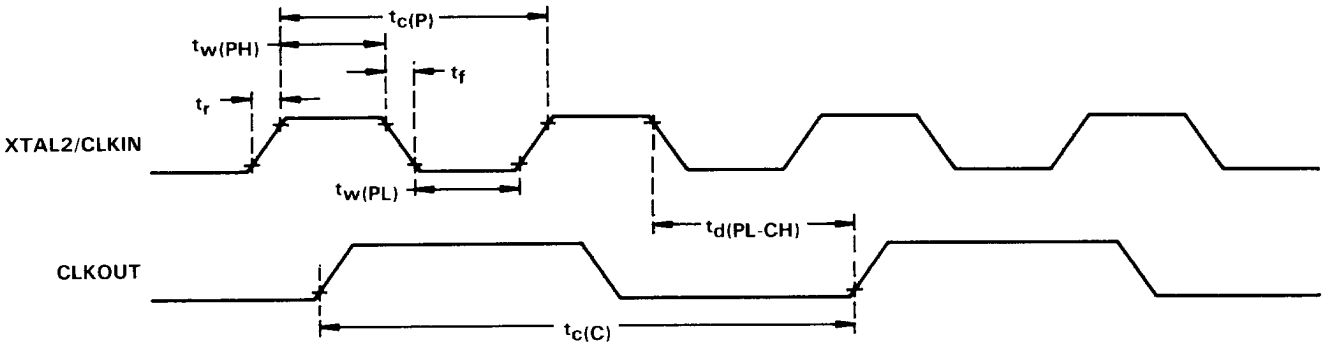
| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current† | Operating mode | $V_{CC}$ = 5.0 V, f = 7.0 MHz | | 17 | 24.5 | mA |
| | | | $V_{CC}$ = 5.0 V, f = 3.0 MHz | | 7.2 | 10.5 | |
| | | | $V_{CC}$ = 5.0 V, f = 0.5 MHz | | 1.2 | 1.8 | |
| | | | $V_{CC}$ = 5.0 V, f = Z MHz | | 2.4Z | 3.5Z | |
| | | | $V_{CC}$ = 2.5 V, f = 0.5 MHz | | 0.4 | 1.2 | |
| | | Wake-up mode 1 (one timer and UART active) | $V_{CC}$ = 5.0 V, f = 7.0 MHz | | 2400 | 5600 | μA |
| | | | $V_{CC}$ = 5.0 V, f = 3.0 MHz | | 1200 | 3300 | |
| | | | $V_{CC}$ = 5.0 V, f = 0.5 MHz | | 250 | 800 | |
| | | Wake-up mode 2 (one timer active and UART off) | $V_{CC}$ = 5.0 V, f = 7.0 MHz | | 960 | 3400 | μA |
| | | | $V_{CC}$ = 5.0 V, f = 3.0 MHz | | 480 | 2000 | |
| | | | $V_{CC}$ = 5.0 V, f = 0.5 MHz | | 140 | 550 | |
| | | Wake-up mode 3 (UART active only) | $V_{CC}$ = 5.0 V, f = 7.0 MHz | | 1500 | 2400 | μA |
| | | | $V_{CC}$ = 5.0 V, f = 3.0 MHz | | 800 | 1500 | |
| | | | $V_{CC}$ = 5.0 V, f = 0.5 MHz | | 180 | 600 | |
| $V_{OH}$ | High-level output voltage ($V_{OH}$ = $V_{IH}$ + 0.4 V) | | $V_{CC}$ = 2.5 V, $I_{OH}$ = −50 μA | 2.25 | 2.4 | | V |
| | | | $V_{CC}$ = 4.0 V, $I_{OH}$ = −0.4 mA | 3.20 | 3.6 | | |
| | | | $V_{CC}$ = 5.0 V, $I_{OH}$ = −0.7 mA | 3.90 | 4.5 | | |
| | | | $V_{CC}$ = 6.0 V, $I_{OH}$ = −1.0 mA | 4.60 | 5.4 | | |
| $V_{OL}$ | Low-level output voltage ($V_{OL}$ = $V_{IL}$ − 0.4 V) | | $V_{CC}$ = 2.5 V, $I_{OL}$ = 0.4 mA | | 0.2 | 0.35 | V |
| | | | $V_{CC}$ = 4.0 V, $I_{OL}$ = 1.6 mA | | 0.4 | 0.80 | |
| | | | $V_{CC}$ = 5.0 V, $I_{OL}$ = 2.5 mA | | 0.6 | 1.10 | |
| | | | $V_{CC}$ = 6.0 V, $I_{OL}$ = 3.4 mA | | 0.8 | 1.40 | |
| $I_{OH}$ | Output source current ($V_{OH}$ = $V_{IH}$ + 0.4 V) | | $V_{CC}$ = 2.5 V, $V_{OH}$ = 2.25 V | −50 | −200 | | μA |
| | | | $V_{CC}$ = 4.0 V, $V_{OH}$ = 3.20 V | −0.4 | −1.4 | | mA |
| | | | $V_{CC}$ = 5.0 V, $V_{OH}$ = 3.90 V | −0.7 | −2.2 | | |
| | | | $V_{CC}$ = 6.0 V, $V_{OH}$ = 4.60 V | −1.0 | −3.3 | | |
| $I_{OL}$ | Output sink current ($V_{OL}$ = $V_{IL}$ − 0.4 V) | | $V_{CC}$ = 2.5 V, $V_{OL}$ = 0.35 V | 0.4 | 0.9 | | mA |
| | | | $V_{CC}$ = 4.0 V, $V_{OL}$ = 0.80 V | 1.6 | 3.5 | | |
| | | | $V_{CC}$ = 5.0 V, $V_{OL}$ = 1.10 V | 2.5 | 5.5 | | |
| | | | $V_{CC}$ = 6.0 V, $V_{OL}$ = 1.40 V | 3.4 | 8.0 | | |
| $I_I$ | Input leakage current | MC | $V_I$ = $V_{SS}$ or $V_{CC}$ | | ±0.1 | ±1 | μA |
| | | All others | $V_I$ = $V_{SS}$ to $V_{CC}$ | | | | |
| $C_I$ | Input capacitance | | | | 5 | | pF |

†All inputs = $V_{CC}$ or $V_{SS}$ (except XTAL2). All I/O and output pins are open circuit.

## recommended crystal operating conditions over full operating range

| PARAMETER | | | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| $f_{osc}$ | Crystal frequency | $V_{CC}$ = 2.5 V | 0.5 | | 0.8 | MHz |
| | | $V_{CC}$ = 4.0 V | 0.5 | | 5.0 | |
| | | $V_{CC}$ = 5.0 V | 0.5 | | 7.0 | |
| | | $V_{CC}$ = 6.0 V | 0.5 | | 7.5 | |
| | CLKIN duty cycle | | 45 | | 55 | % |
| $t_{c(P)}$ | Crystal cycle time | $V_{CC}$ = 2.5 V | 1250 | | 2000 | ns |
| | | $V_{CC}$ = 4.0 V | 200 | | 2000 | |
| | | $V_{CC}$ = 5.0 V | 143 | | 2000 | |
| | | $V_{CC}$ = 6.0 V | 133 | | 2000 | |
| $t_{c(C)}$ | Internal state cycle time | $V_{CC}$ = 2.5 V | 2500 | | 4000 | ns |
| | | $V_{CC}$ = 4.0 V | 400 | | 4000 | |
| | | $V_{CC}$ = 5.0 V | 286 | | 4000 | |
| | | $V_{CC}$ = 6.0 V | 267 | | 4000 | |
| $t_{w(PH)}$ | CLKIN pulse duration high | | 50 | | | ns |
| $t_{w(PL)}$ | CLKIN pulse duration low | | 50 | | | ns |
| $t_r$ | CLKIN rise time | | | | 30 | ns |
| $t_f$ | CLKIN fall time | | | | 30 | ns |
| $t_{d(PL-CH)}$ | CLKIN fall to CLKOUT rise delay time | | | 140 | 250 | ns |

## clock timing



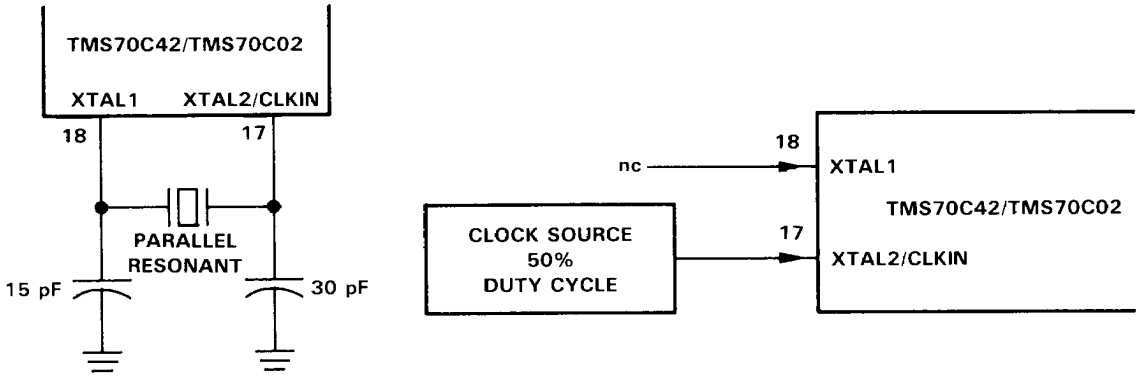




FIGURE 19. RECOMMENDED CLOCK CONNECTIONS

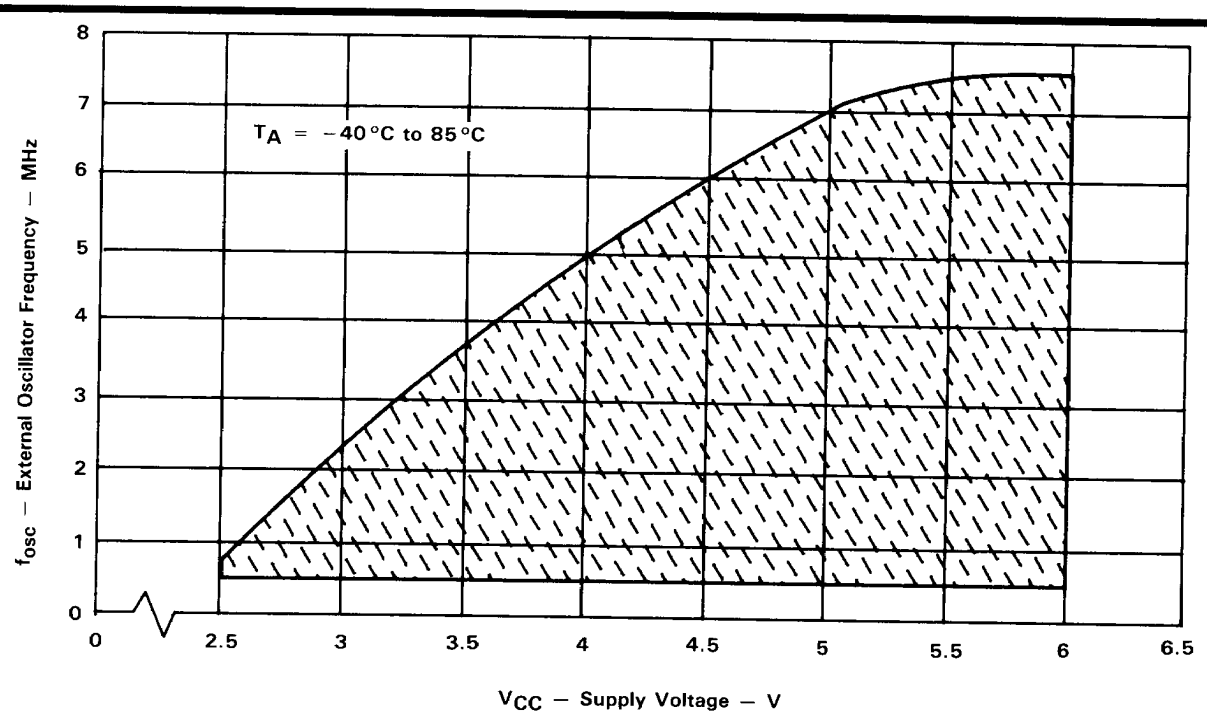



FIGURE 20. OPERATING FREQUENCY RANGE

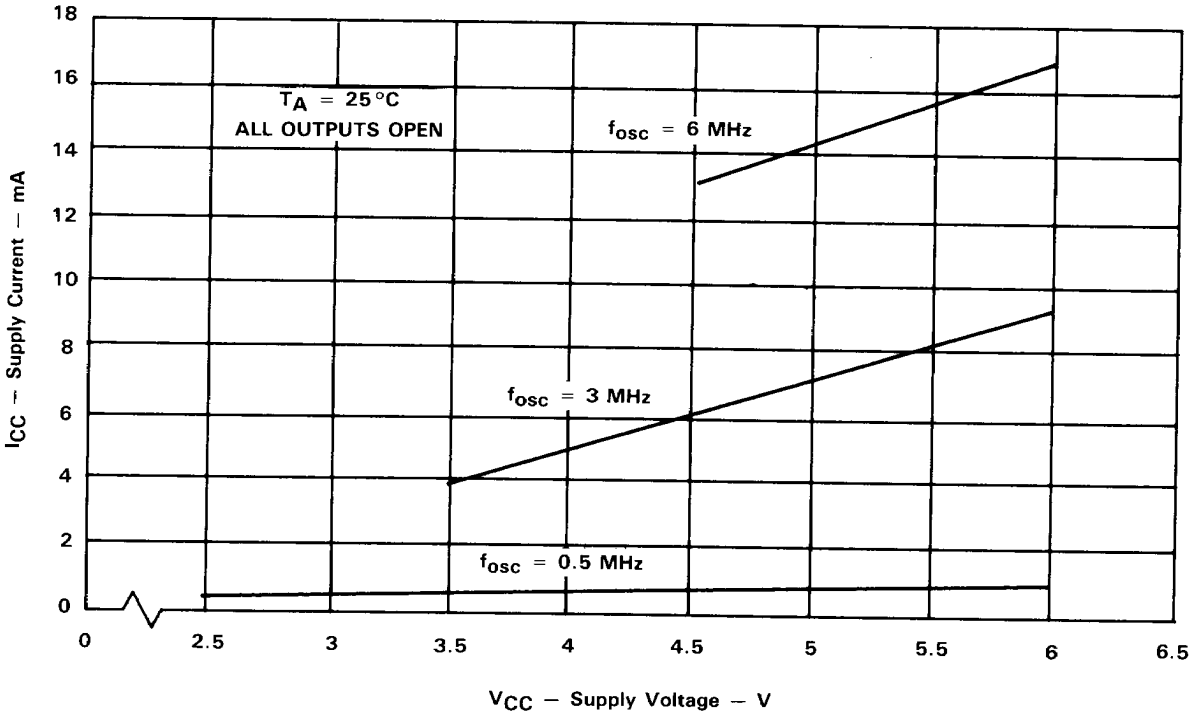



FIGURE 21. TYPICAL OPERATING CURRENT VS. SUPPLY VOLTAGE



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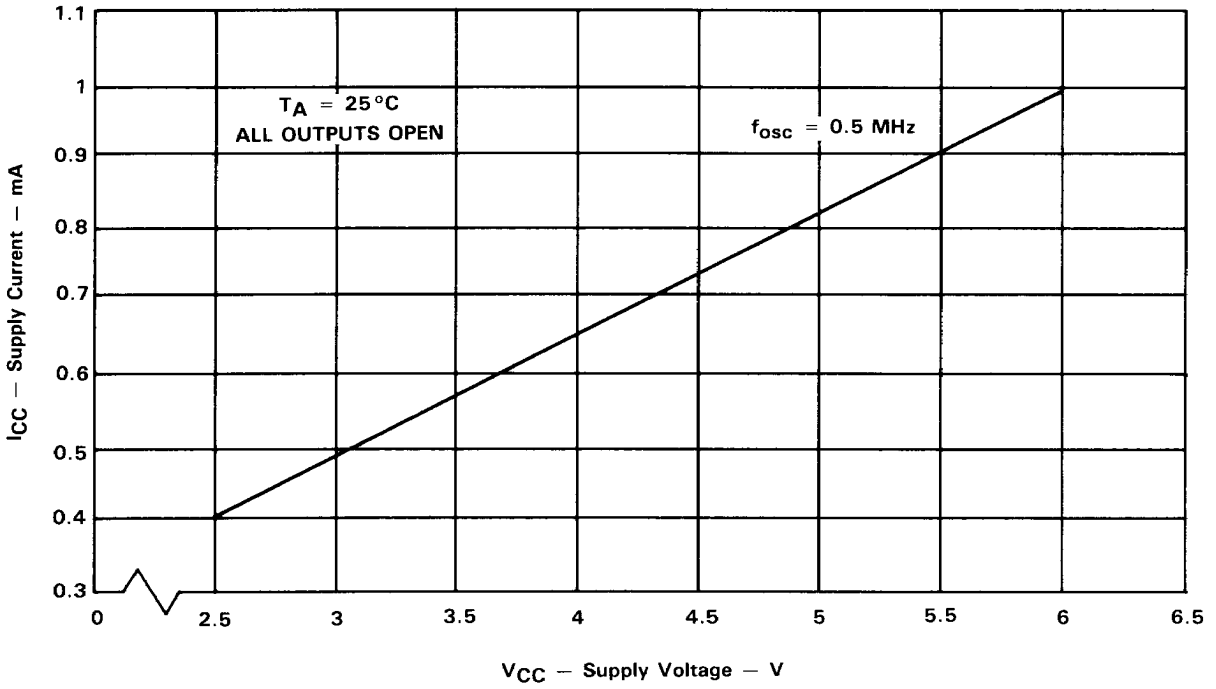


FIGURE 22. TYPICAL OPERATING CURRENT VS. SUPPLY VOLTAGE

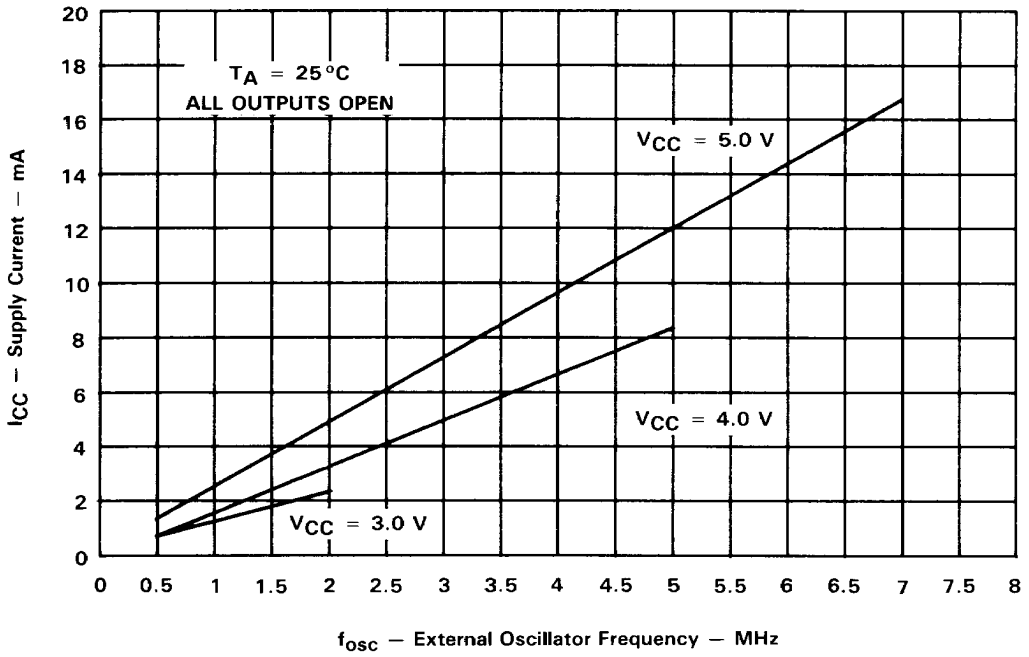


FIGURE 23. TYPICAL OPERATING $I_{CC}$ VS. OSCILLATOR FREQUENCY

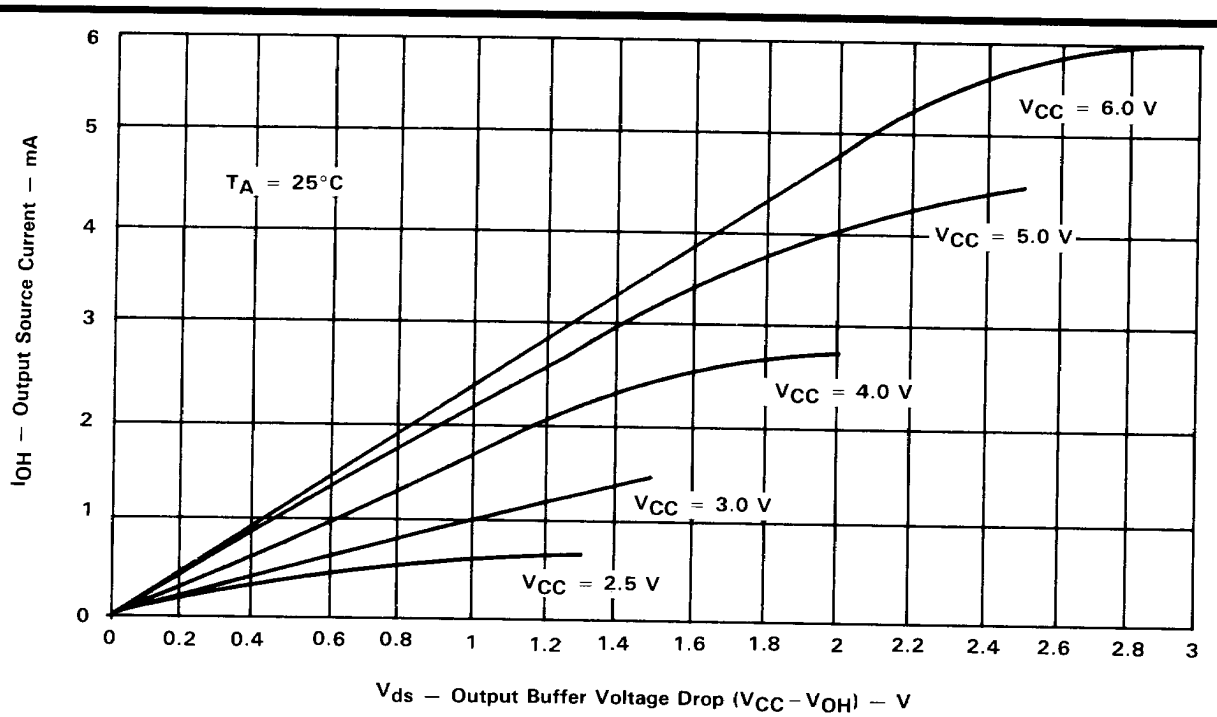


FIGURE 24. TYPICAL OUTPUT SOURCE CHARACTERISTICS

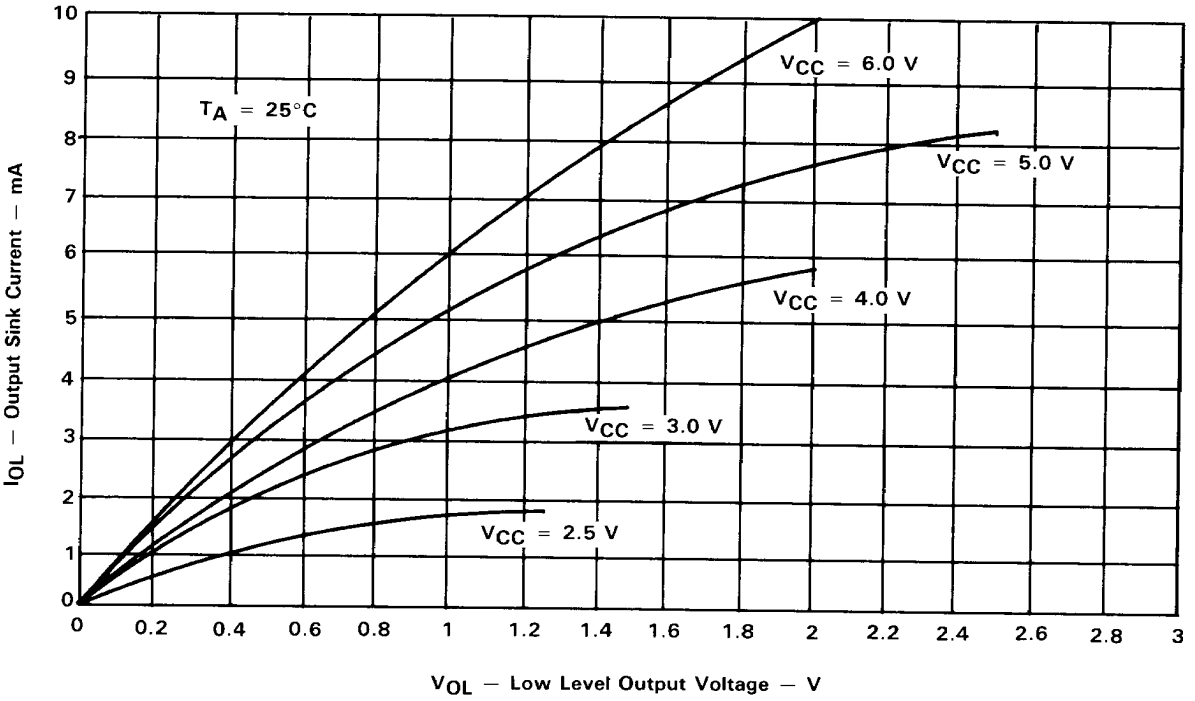


FIGURE 25. TYPICAL OUTPUT SINK CHARACTERISTICS



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## 5 VOLTS ± 10% CMOS SPECIFICATION

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 6) . . . . . −0.3 V to 7 V
Input voltage range . . . . . −0.3 V to $V_{CC}$ +0.3 V
Output voltage range . . . . . −0.3 V to $V_{CC}$ +0.3 V
Maximum I/O buffer current . . . . . ±10 mA
Maximum supply current, $I_{CC}$ . . . . . 60 mA
Maximum supply current, $I_{SS}$ . . . . . −60 mA
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: All voltage values in this data sheet are with respect to $V_{SS}$.

### recommended operating conditions

| | | | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | | 5.5 | V |
| $V_{IH}$ | High-level input voltage | All inputs except MC, XTAL2 | 0.7 $V_{CC}$ | | | V |
| | | MC, XTAL2 | 0.8 $V_{CC}$ | | | |
| $V_{IL}$ | Low-level input voltage | All inputs except MC, XTAL2 | | | 0.3 $V_{CC}$ | V |
| | | MC, XTAL2 | | | 0.2 $V_{CC}$ | |
| $T_A$ | Operating free-air temperature | Commercial (TMS70C42NL) | 0 | | 70 | °C |
| | | Industrial (TMS70C42NA) | −40 | | 85 | |

## electrical characteristics over full range of operating conditions ($V_{CC}$ = 4.5 V to 5.5 V)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current‡ | Operating mode | f = 6.0 MHz | | 15 | 24 | mA |
| | | | f = 3.0 MHz | | 7.2 | 12 | |
| | | | f = 1.0 MHz | | 2.4 | 4.0 | |
| | | | f = Z MHz | | 2.4Z | 4.0Z | |
| | | Wake-up mode 1 (one timer and UART active) | f = 6.0 MHz | | 2400 | 5400 | μA |
| | | | f = 3.0 MHz | | 1200 | 2900 | |
| | | | f = 1.0 MHz | | 650 | 1500 | |
| | | Wake-up mode 2 (one timer active and UART off) | f = 6.0 MHz | | 960 | 3200 | μA |
| | | | f = 3.0 MHz | | 480 | 1800 | |
| | | | f = 1.0 MHz | | 350 | 1000 | |
| | | Wake-up mode 3 (UART active only) | f = 6.0 MHz | | 1500 | 2200 | μA |
| | | | f = 3.0 MHz | | 800 | 1300 | |
| | | | f = 1.0 MHz | | 400 | 1100 | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = 0.3 mA | $V_{CC}$−0.5 V | 4.7 | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 1.4 mA | | 0.2 | 0.4 | V |
| $I_{OH}$ | High-level output source current | | $V_{OH}$ = $V_{CC}$ −0.5 V | −0.3 | −1.2 | | mA |
| | | | $V_{OH}$ = 2.5 V min. | −1.0 | −3.0 | | |
| $I_{OL}$ | Output sink current | | $V_{OL}$ = 0.4 V | 1.4 | 2.0 | | mA |
| $I_I$ | Input leakage current | MC | $V_I$ = $V_{SS}$ or $V_{CC}$ | | ±0.1 | ±1.0 | μA |
| | | All others | $V_I$ = $V_{SS}$ to $V_{CC}$ | | | | |
| $C_I$ | Input capacitance | | | | 5 | | pF |

†Typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡All inputs = $V_{CC}$ or $V_{SS}$ (except XTAL2). All I/O and output pins are open circuit.

## AC characteristics for input/output ports†

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{r(IO)}$ | I/O port output rise time | $C_L$ = 15 pF, $V_{CC}$ = 5 V | | 35 | 60 | ns |
| $t_{f(IO)}$ | I/O port output fall time | $C_L$ = 15 pF, $V_{CC}$ = 5 V | | 20 | 50 | ns |

†Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points.

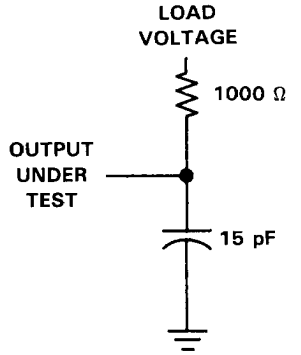


**FIGURE 26. OUTPUT LOAD CIRCUIT USED FOR ALL TIMING MEASUREMENTS**



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## recommended crystal operating conditions over full operating range

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{osc}$ | Crystal frequency | 0.5 | | 6.0 | MHz |
| | CLKIN duty cycle | 45 | | 55 | % |
| $t_{c(P)}$ | Crystal cycle time | 167 | | 2000 | ns |
| $t_{c(C)}$ | Internal state cycle time | 333 | | 4000 | ns |
| $t_{w(PH)}$ | CLKIN pulse duration high | 50 | | | ns |
| $t_{w(PL)}$ | CLKIN pulse duration low | 50 | | | ns |
| $t_r$ | CLKIN rise time | | | 30 | ns |
| $t_f$ | CLKIN fall time | | | 30 | ns |
| $t_{d(PL-CH)}$ | CLKIN fall to CLKOUT rise delay | | 140 | 250 | ns |

## clock timing

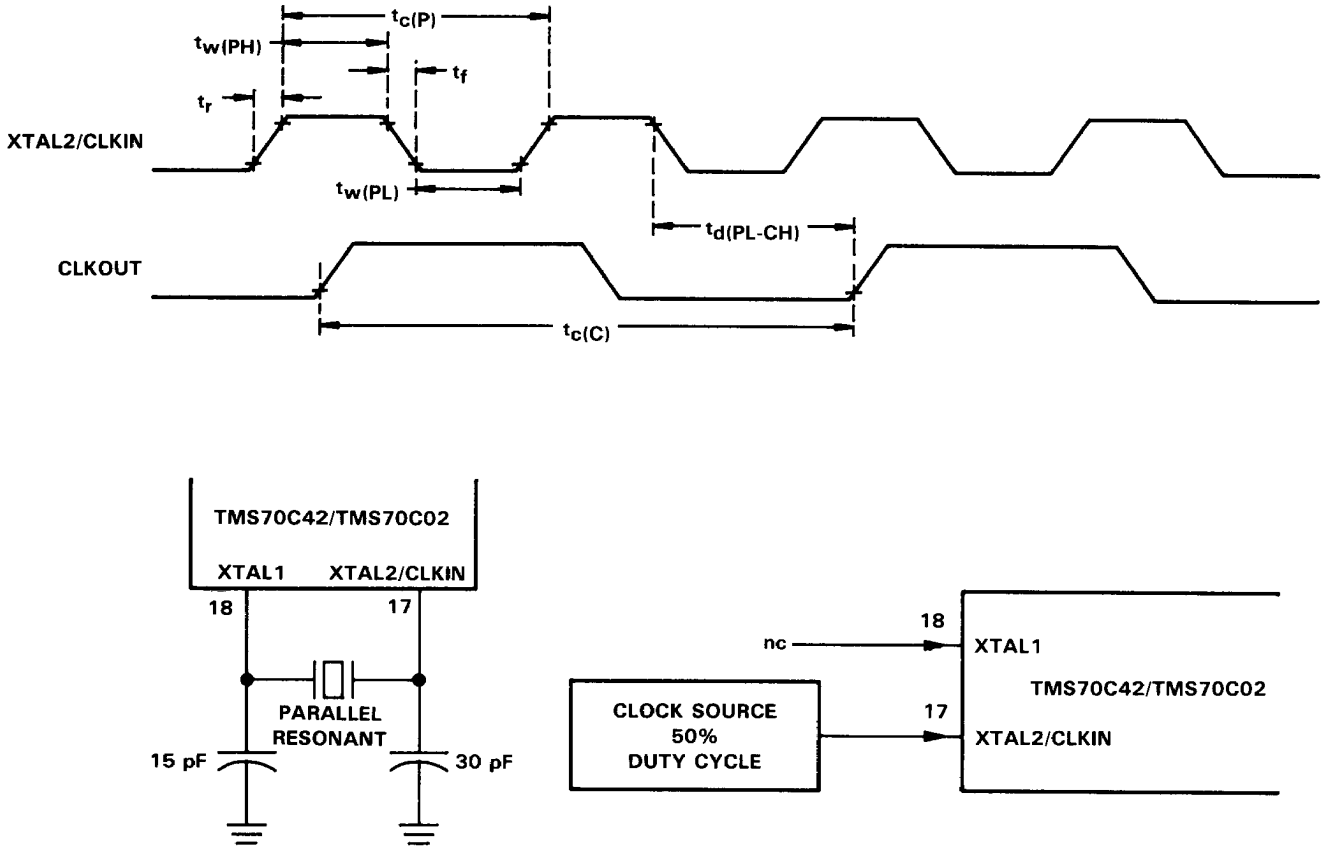


FIGURE 27. RECOMMENDED CLOCK CONNECTIONS

### memory interface timing as a function of frequency

In the table below, $t_{c(C)}$ is the period of the internal clock, and $t_{c(C)} = 2/f_{osc}$. At 6 MHz $t_{c(C)}$ would be 333 ns. Minimum and maximum times may be calculated by using the formulas below with the appropriate clock period.

| | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c(C)}$ | CLKOUT cycle time (see Note 7) | 333 | | 4000 | ns |
| $t_{w(CH)}$ | CLKOUT high pulse duration | $0.5t_{c(C)}-90$ | $0.5t_{c(C)}$ | $0.5t_{c(C)}+90$ | ns |
| $t_{w(CL)}$ | CLKOUT low pulse duration | $0.5t_{c(C)}-90$ | $0.5t_{c(C)}$ | $0.5t_{c(C)}+90$ | ns |
| $t_{d(CH-JL)}$ | Delay time, CLKOUT rise to ALATCH fall | $0.5t_{c(C)}-50$ | $0.5t_{c(C)}$ | | ns |
| $t_{w(JH)}$ | ALATCH high pulse duration | $0.25t_{c(C)}-50$ | $0.25t_{c(C)}$ | | ns |
| $t_{su(HA-JL)}$ | Setup time, high address valid before ALATCH fall | $0.25t_{c(C)}-45$ | $0.25t_{c(C)}$ | | ns |
| $t_{su(LA-JL)}$ | Setup time, low address valid before ALATCH fall | $0.25t_{c(C)}-45$ | $0.25t_{c(C)}$ | | ns |
| $t_{h(JL-LA)}$ | Hold time, low address valid after ALATCH fall | $0.5t_{c(C)}-35$ | $0.5t_{c(C)}$ | | ns |
| $t_{su(RW-JL)}$ | Setup time, R/$\overline{W}$ valid before ALATCH fall | $0.25t_{c(C)}-40$ | $0.25t_{c(C)}$ | | ns |
| $t_{h(EH-RW)}$ | Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise | $0.5t_{c(C)}-60$ | $0.5t_{c(C)}$ | | ns |
| $t_{h(EH-HA)}$ | Hold time, high address valid after $\overline{ENABLE}$ rise | $0.5t_{c(C)}-60$ | $0.5t_{c(C)}$ | | ns |
| $t_{su(Q-EH)}$ | Setup time, data output valid before $\overline{ENABLE}$ rise | $0.5t_{c(C)}-70$ | $0.5t_{c(C)}$ | | ns |
| $t_{h(EH-Q)}$ | Hold time, data output valid after $\overline{ENABLE}$ rise | $0.5t_{c(C)}-60$ | $0.5t_{c(C)}$ | | ns |
| $t_{d(LA-EL)}$ | Delay time, low address high impedance to $\overline{ENABLE}$ fall | $0.25t_{c(C)}-45$ | $0.25t_{c(C)}$ | | ns |
| $t_{d(EH-A)}$ | Delay time, $\overline{ENABLE}$ rise to next address drive | $0.5t_{c(C)}-60$ | $0.5t_{c(C)}$ | | ns |
| $t_{a(EL-D)}$ | Access time, data input valid after $\overline{ENABLE}$ fall | $0.75t_{c(C)}-160$ | $0.75t_{c(C)}$ | | ns |
| $t_{a(A-D)}$ | Access time, address valid to data input valid | $1.5t_{c(C)}-200$ | $1.5t_{c(C)}-100$ | | ns |
| $t_{d(A-EH)}$ | Delay time, address valid to $\overline{ENABLE}$ rise | $1.5t_{c(C)}-50$ | $1.5t_{c(C)}$ | | ns |
| $t_{h(EH-D)}$ | Hold time, data input valid after $\overline{ENABLE}$ rise | 0 | | | ns |
| $t_{d(EH-JH)}$ | Delay time, $\overline{ENABLE}$ rise to ALATCH rise | $0.5t_{c(C)}-60$ | $0.5t_{c(C)}$ | | ns |
| $t_{d(CH-EL)}$ | Delay time, CLKOUT rise to $\overline{ENABLE}$ fall | | 30 | | ns |

NOTE 7: $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

As an example, consider calculating the minimum data out hold time from $\overline{ENABLE}$ rising [$t_{h(EH-Q)}$]. At 6MHz this would give:

$$t_{h(EH-Q)} = 0.5t_{c(C)} - 60 \text{ ns}$$
$$= 0.5(333 \text{ ns}) - 60 \text{ ns}$$
$$= 166.5 \text{ ns} - 60 \text{ ns}$$
$$\therefore t_{h(EH-Q)} = 106.5 \text{ ns}$$



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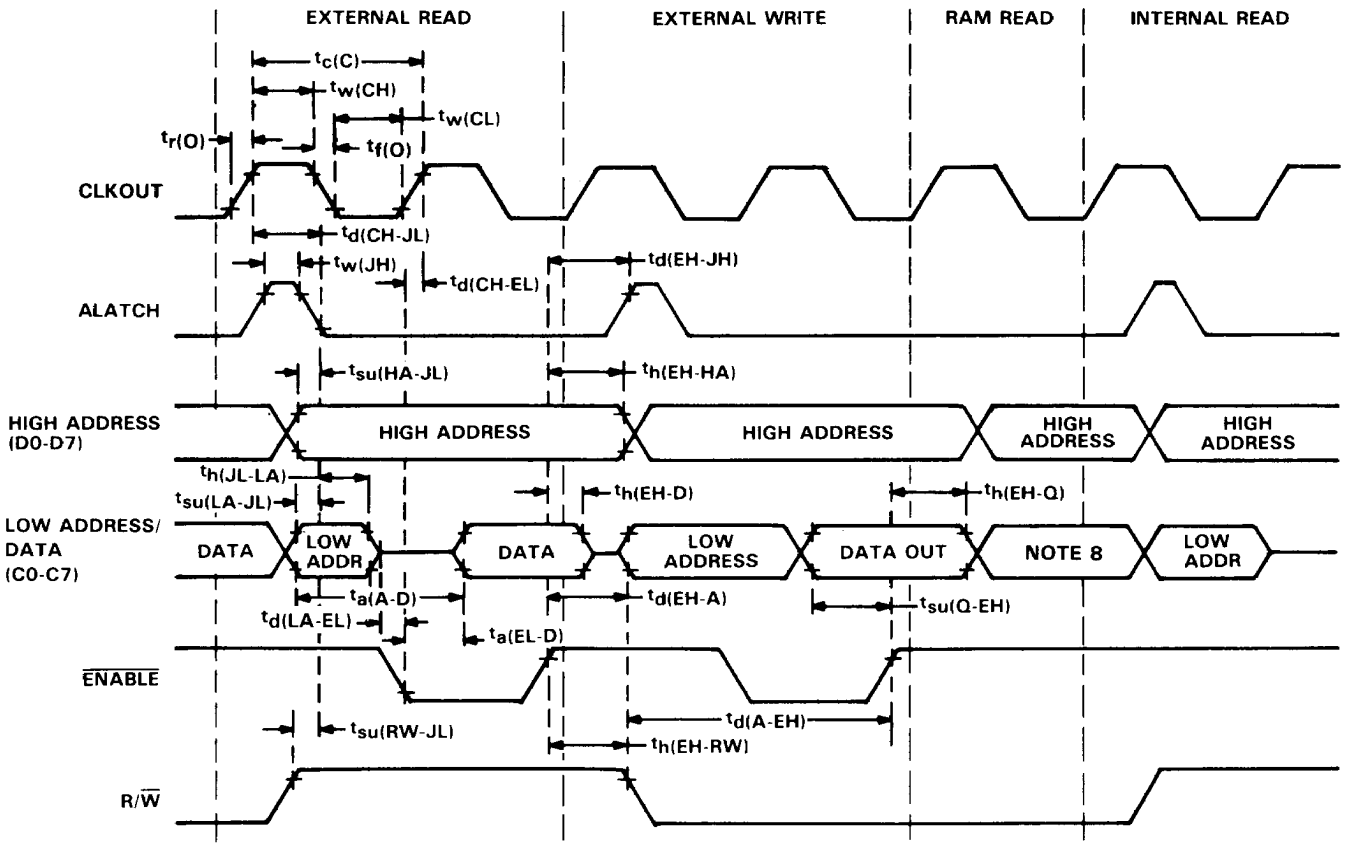
## memory interface timing at 6 MHz

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{c(C)}$ | CLKOUT cycle time (see Note 7) | f = 6 MHz<br>duty cycle = 50%<br>$V_{CC}$ = 4.5 V to 5.5 V | | 333 | | ns |
| $t_{w(CH)}$ | CLKOUT high pulse duration | | 76 | 166 | 252 | ns |
| $t_{w(CL)}$ | CLKOUT low pulse duration | | 76 | 162 | 252 | ns |
| $t_{d(CH-JL)}$ | Delay time, CLKOUT rise to ALATCH fall | | 116 | 166 | | ns |
| $t_{w(JH)}$ | ALATCH high pulse duration | | 33 | 83 | | ns |
| $t_{su(HA-JL)}$ | Setup time, high address valid before ALATCH fall | | 38 | 83 | | ns |
| $t_{su(LA-JL)}$ | Setup time, low address valid before ALATCH fall | | 38 | 83 | | ns |
| $t_{h(JL-LA)}$ | Hold time, low address valid after ALATCH fall | | 131 | 166 | | ns |
| $t_{su(RW-JL)}$ | Setup time, R/$\overline{W}$ valid before ALATCH fall | | 43 | 83 | | ns |
| $t_{h(EH-RW)}$ | Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise | | 106 | 166 | | ns |
| $t_{h(EH-HA)}$ | Hold time, high address valid after $\overline{ENABLE}$ rise | | 106 | 166 | | ns |
| $t_{su(Q-EH)}$ | Setup time, data output valid before $\overline{ENABLE}$ rise | | 96 | 166 | | ns |
| $t_{h(EH-Q)}$ | Hold time, data output valid after $\overline{ENABLE}$ rise | | 106 | 166 | | ns |
| $t_{d(LA-EL)}$ | Delay time, low address high impedance to $\overline{ENABLE}$ fall | | 38 | 83 | | ns |
| $t_{d(EH-A)}$ | Delay time, $\overline{ENABLE}$ rise to next address drive | | 106 | 166 | | ns |
| $t_{a(EL-D)}$ | Access time, data input valid after $\overline{ENABLE}$ fall | | 90 | 250 | | ns |
| $t_{a(A-D)}$ | Access time, address valid to data input valid | | 300 | 400 | | ns |
| $t_{d(A-EH)}$ | Delay time, address valid to $\overline{ENABLE}$ rise | | 450 | 500 | | ns |
| $t_{h(EH-D)}$ | Hold time, data input valid after $\overline{ENABLE}$ rise | | 0 | | | ns |
| $t_{d(EH-JH)}$ | Delay time, $\overline{ENABLE}$ rise to ALATCH rise | | 106 | 166 | | ns |
| $t_{d(CH-EL)}$ | Delay time, CLKOUT rise to $\overline{ENABLE}$ fall | | | 30 | | ns |

NOTE 7: $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

## read and write cycle timing




NOTE 8: During an internal RAM access, the CPORT outputs are stable but the data is a "don't care".



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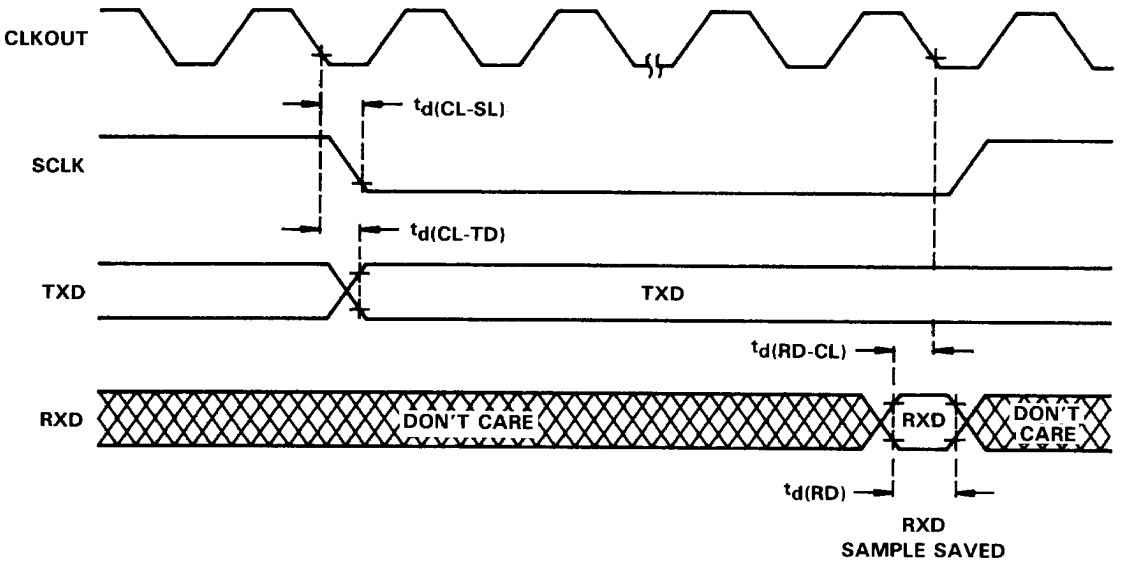
## serial port timing

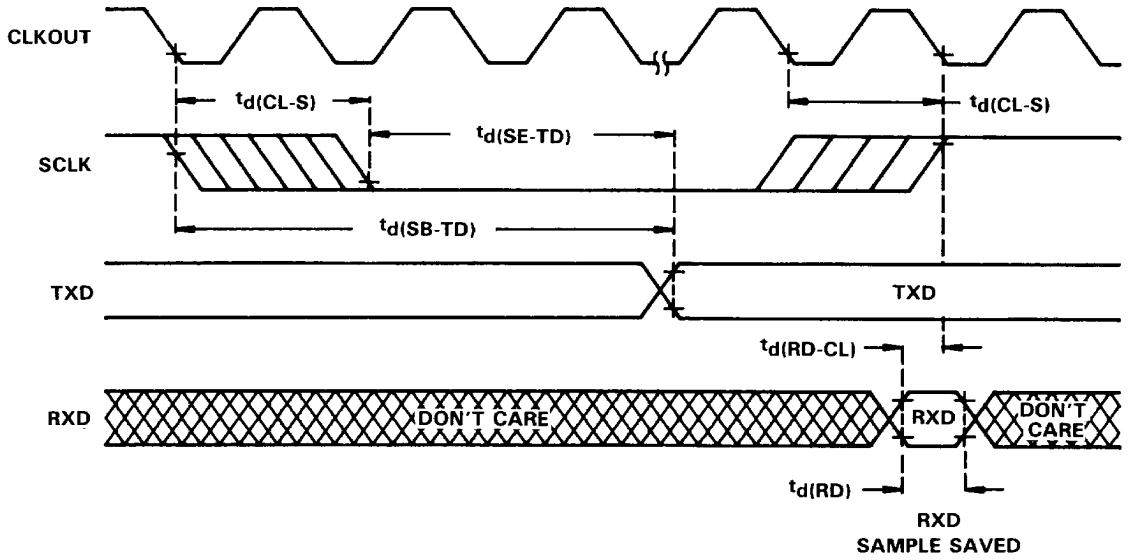
### internal serial clock




NOTES: 9. The CLKOUT signal is not available in Single-Chip mode.
10. CLKOUT = $t_{c(C)} = \phi$.
11. SCLK = $\phi/8$ in this example.

| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $t_{d(CL-SL)}$ | CLKOUT low to SCLK low | 1/4 $t_{c(C)}$ | ns |
| $t_{d(CL-TD)}$ | CLKOUT low to new TXD data | 1/4 $t_{c(C)}$ | ns |
| $t_{d(RD-CL)}$ | RXD data valid before CLKOUT low | 1/4 $t_{c(C)}$ | ns |
| $t_{d(RD)}$ | RXD data valid time | 1/2 $t_{c(C)}$ | ns |

**external serial clock**




NOTES: 12. The CLKOUT signal is not available in Single-Chip mode.
13. CLKOUT = $t_{c(C)} = \phi$.
14. SCLK = $\phi/8$ in this example.
15. SCLK sampled; if SCLK = 1 then 0, fall transition found.
16. SCLK sampled; if SCLK = 0 then 1, rise transition found.

| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $t_{d(RD-CL)}$ | RXD data valid before CLKOUT low | 1/4 $t_{c(C)}$ | ns |
| $t_{d(RD)}$ | RXD data valid time | 1/2 $t_{c(C)}$ | ns |
| $t_{d(SB-TD)}$ | Start of SCLK sample to new TXD data | 3 1/4 $t_{c(C)}$ | ns |
| $t_{d(SE-TD)}$ | End of SCLK sample to new TXD data | 2 1/4 $t_{c(C)}$ | ns |
| $t_{d(CL-S)}$ | CLKOUT low to SCLK transition | $t_{c(C)}$ | ns |



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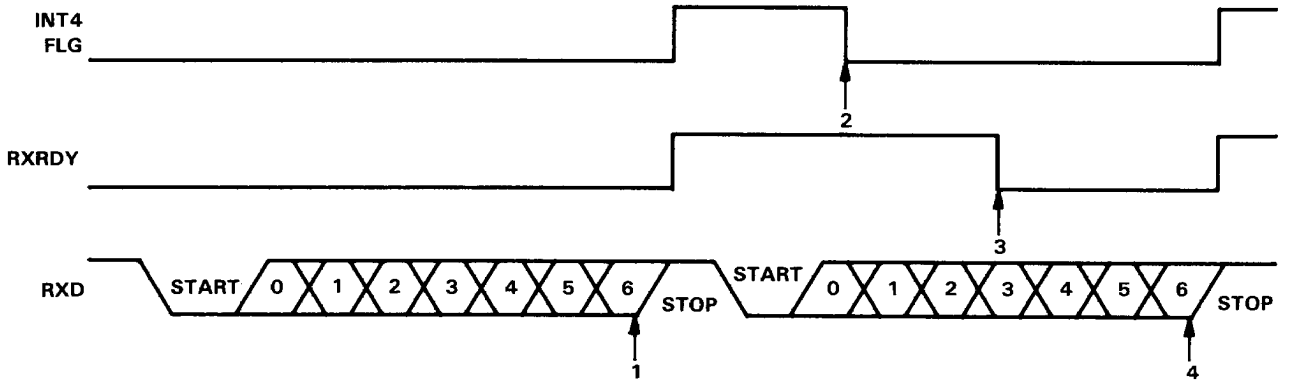
**RX signals in communication modes**

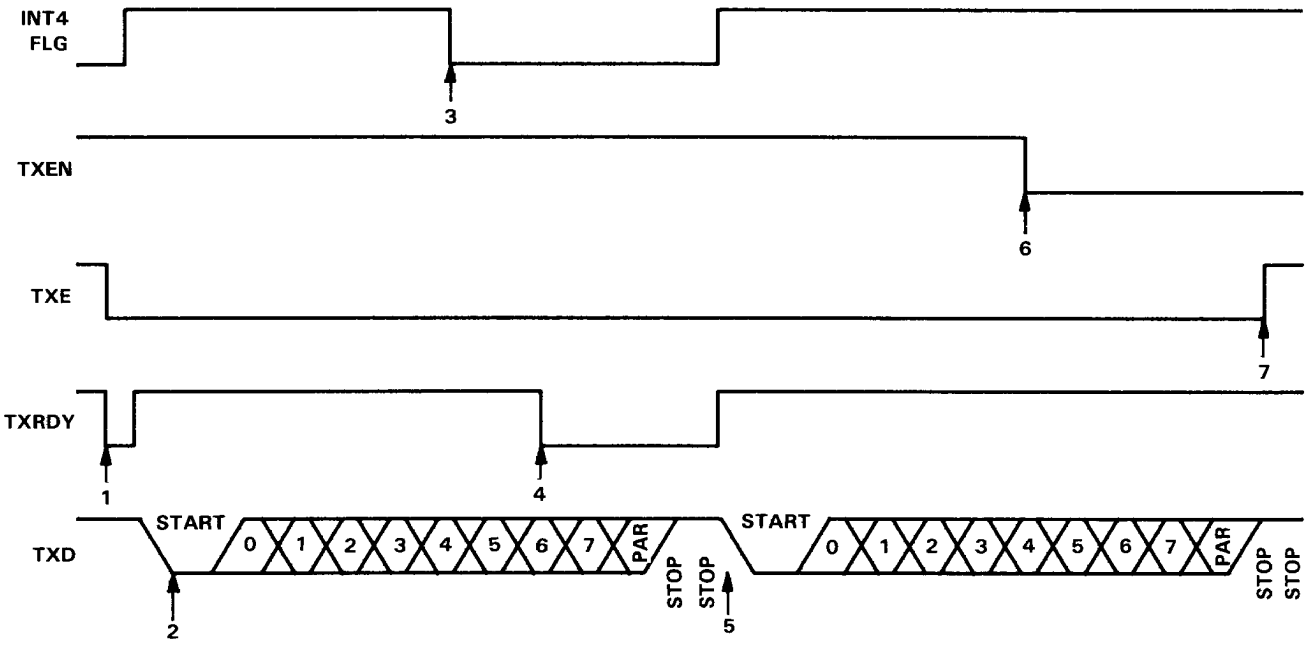



NOTES: 17. Format shown is start bit + seven data bits + stop bit.
18. SCLK is continuous, external or internal.
19. If RXEN = 0, RXSHF still receives data from RXD. However, the data is not transferred to RXBUF and RXRDY and INT4FLG are not set.

**Sequence of Events:**

1. RXSHF data is transferred to RXBUF. Error status bits are set if an error is detected.
2. Software writes to INT4CLR to clear INT4FLG. If not, CPU clears.
3. INT4FLG on entry to level 4 interrupt routine.
4. Software reads RXBUF.

**TX signals in comunications modes**

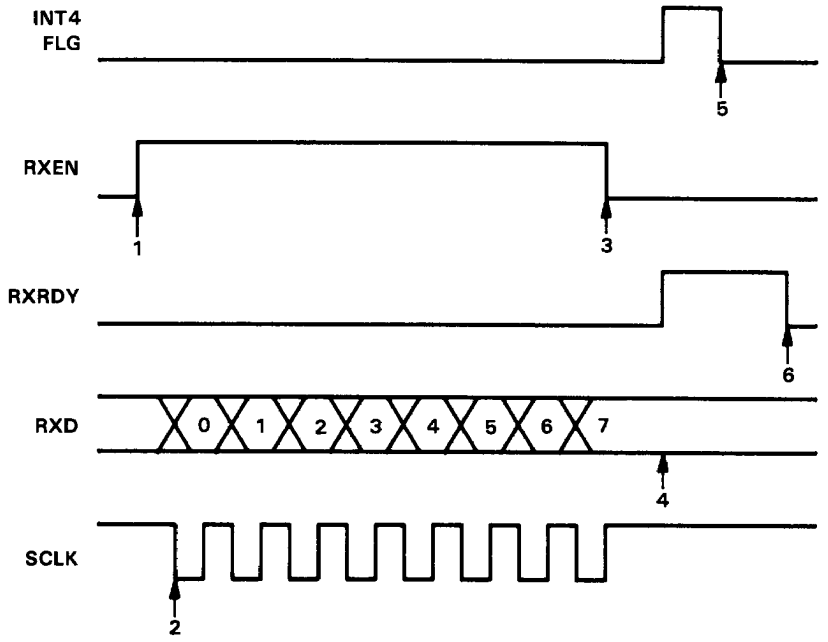



NOTES: 20. Format shown is start bit + eight data bits + parity bit + two stop bits.
21. SCLK is continuous whether internal or external.

**Sequence of Events:**

1. Software writes to TXBUF.
2. TXBUF and WU data are transferred to TXSHF and WUT (Wake-up temporary flag). INT4FLG and TXRDY are set.
3. Software writes to INT4CLR to clear INT4FLG or CPU clears INT4FLG on entry to level 4 interrupt routine.
4. Software writes to TXBUF.
5. Software writes to INT4CLR to clear INT4FLG or CPU clears INT4FLG on entry to level 4 interrupt routine.
6. Software resets TXEN; current frame will finish and transmission will stop whether TXBUF is full or empty.
7. TXE is set if TXBUF and TXSFT are empty.

**RX signals in serial I/O modes**




NOTES: 22. RXEN has no effect on INT4FLG or RXRDY in Serial I/O mode.
23. RXD is sampled on SCLK rise; external shift registers should be clocked on SCLK fall.
24. The SCLK source should be internal as it is gated by internal circuitry.

**Sequence of Events:**

1. Software starts receiving by setting RXEN.
2. Gated SCLK starts and data is received.
3. RXEN is automatically cleared in last data bit.
4. RXSHF data is transferred to RXBUF, and RXRDY and INT4 are set.
5. Software writes to INT4CLR to clear INT4FLG; if not, CPU clears INT4FLG on entry to level 4 interrupt routine.
6. Software reads RXBUF.



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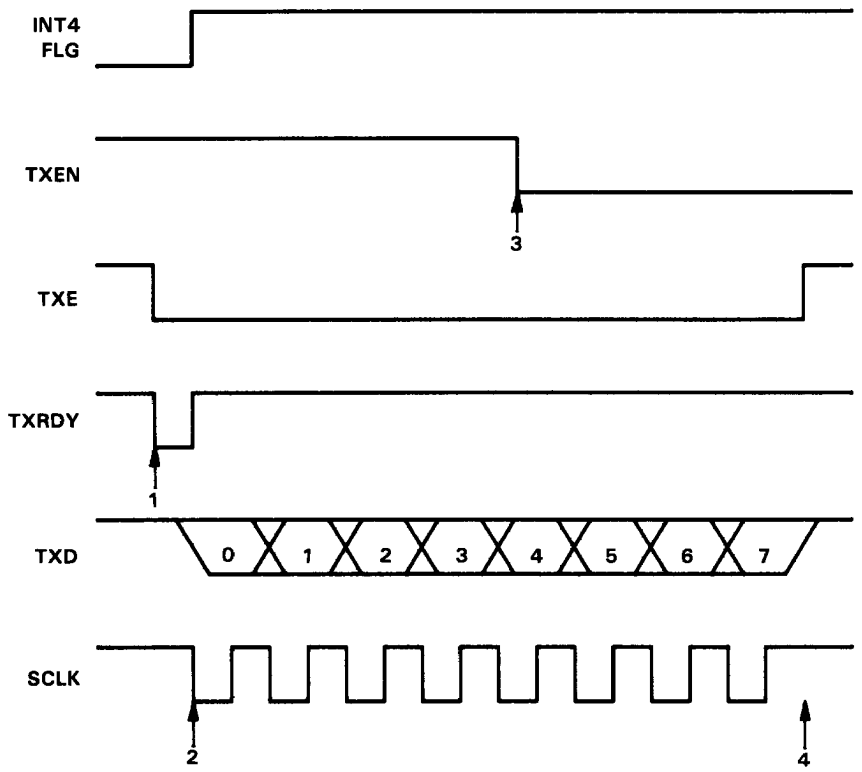
**TX signals in serial I/O modes**



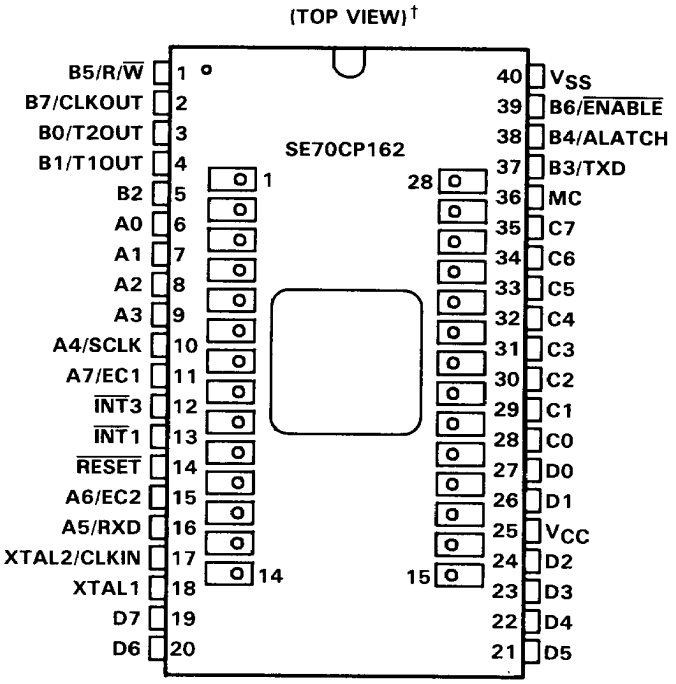

NOTES: 25. Format shown is eight data bits.
26. The SCLK sources should be internal as it is gated by internal circuitry.

**Sequence of Events:**

1. Software writes to TXBUF.
2. TXBUF data is transferred to TXSFT; INT4FLG and TXRDY are set, and SCLK starts.
3. Software resets TXEN, current frame will finish and transmission will halt whether TXBUF is full or empty.
4. Frame ends and SCLK stops because TXEN = 0.

## SE70CP162

The SE70CP162 is a prototyping device for the TMS70C42. The SE70CP162 can accommodate up to 16K bytes of EPROM and is packaged so that a standard 2764, 27C64, 27128, or 27C128 EPROM can be plugged into the socket on top (piggyback). It is designed to be used in the prototyping environment and is tested and supported for that purpose. Texas Instruments does not support or warrant the use of the SE70CP162 for production.




†SE70CP162 pin spacing is standard for 40-pin DIP package.

**FIGURE 28. SE70CP162 PROTOTYPING DEVICE**

All features, performance, and functions are the same as for the TMS70C42 except:

- Operating voltage range (2.5 to 6.0 V) restrictions apply to EPROM voltages
- Power consumption = TMS70C42 power plus EPROM power consumption
- Temperature range = 0 to 55 °C
- Requires standard 250 ns EPROM



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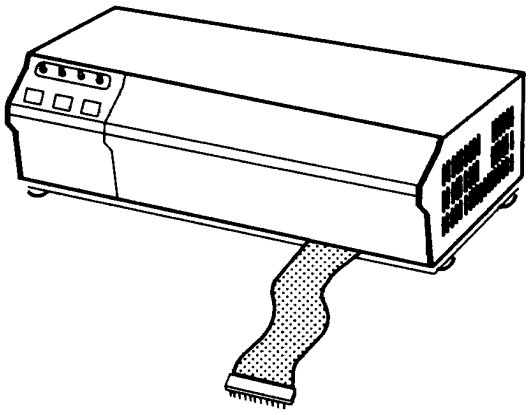
## TMS70C42 DEVELOPMENT SUPPORT

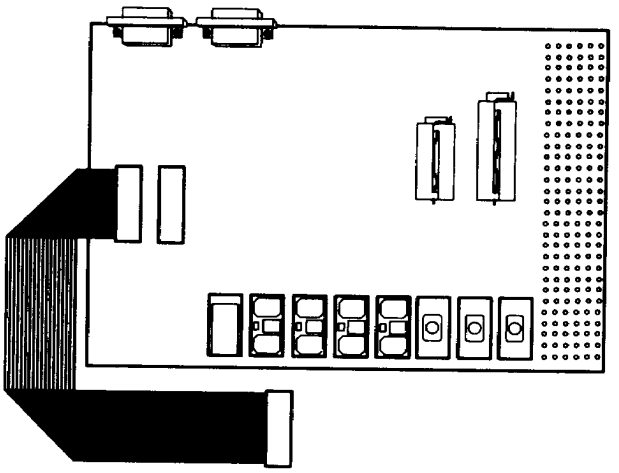
### XDS* — extended development system



- Full TMS7000 Family Development System
- Host Independent/RS-232-C Interface
- Full Speed In-Circuit Emulation
- Extensive Breakpoint and Trace Functions
  - —Detailed Timing Analysis
  - —2K-Byte Trace Samples
  - —Breakpoint Sequencing Ability
- Command/Default Storage
- Removable Target Connector
- External Probe for Breakpoint/ Trace Qualifiers
- On-Board Assembler and Reverse Assembler
- Multiprocessing Capabilities

### EVM — evaluation module

- TMS7000 Family Low Cost Development System
- Single-Chip Mode Emulation Only
- On-Board Assembler/Line Text Editor
- On-Board Hardware/Software Debugger
- Multiple Breakpoints
- Trace Display Function
- EPROM Programmer Utilities
- NMOS and CMOS versions



### assembler/linker packages

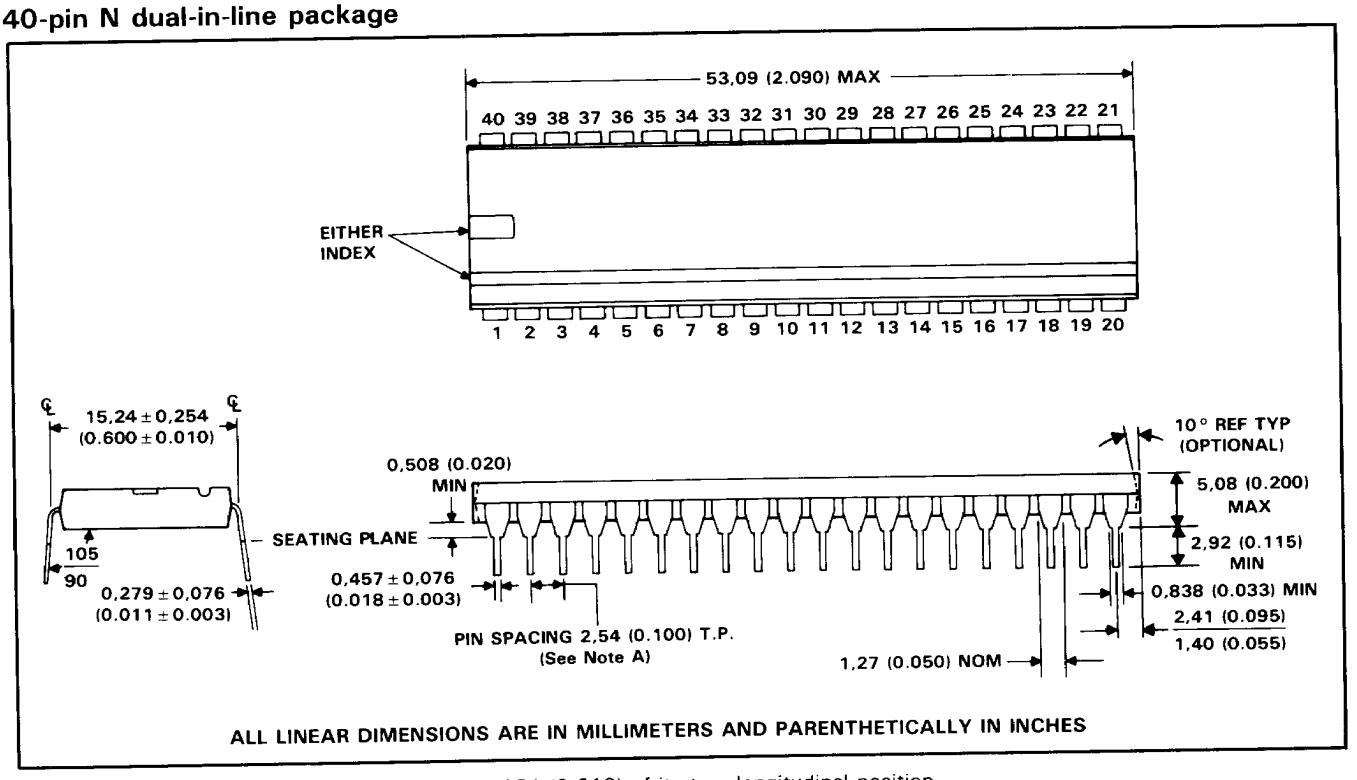
Crossware* assembler/linker packages are available through Texas Instruments for the following operating systems:

| Operating System | TI Part Number |
|---|---|
| TI and IBM PC | TMDS7040810-02 |
| DEC VAX VMS | TMDS7040210-08 |
| IBM MVS | TMDS7040310-08 |
| IBM CMS | TMDS7040320-08 |

*XDS and Crossware are registered trademarks of Texas Instruments Incorporated.

## MECHANICAL DATA

### 40-pin N dual-in-line package




NOTE A: Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.



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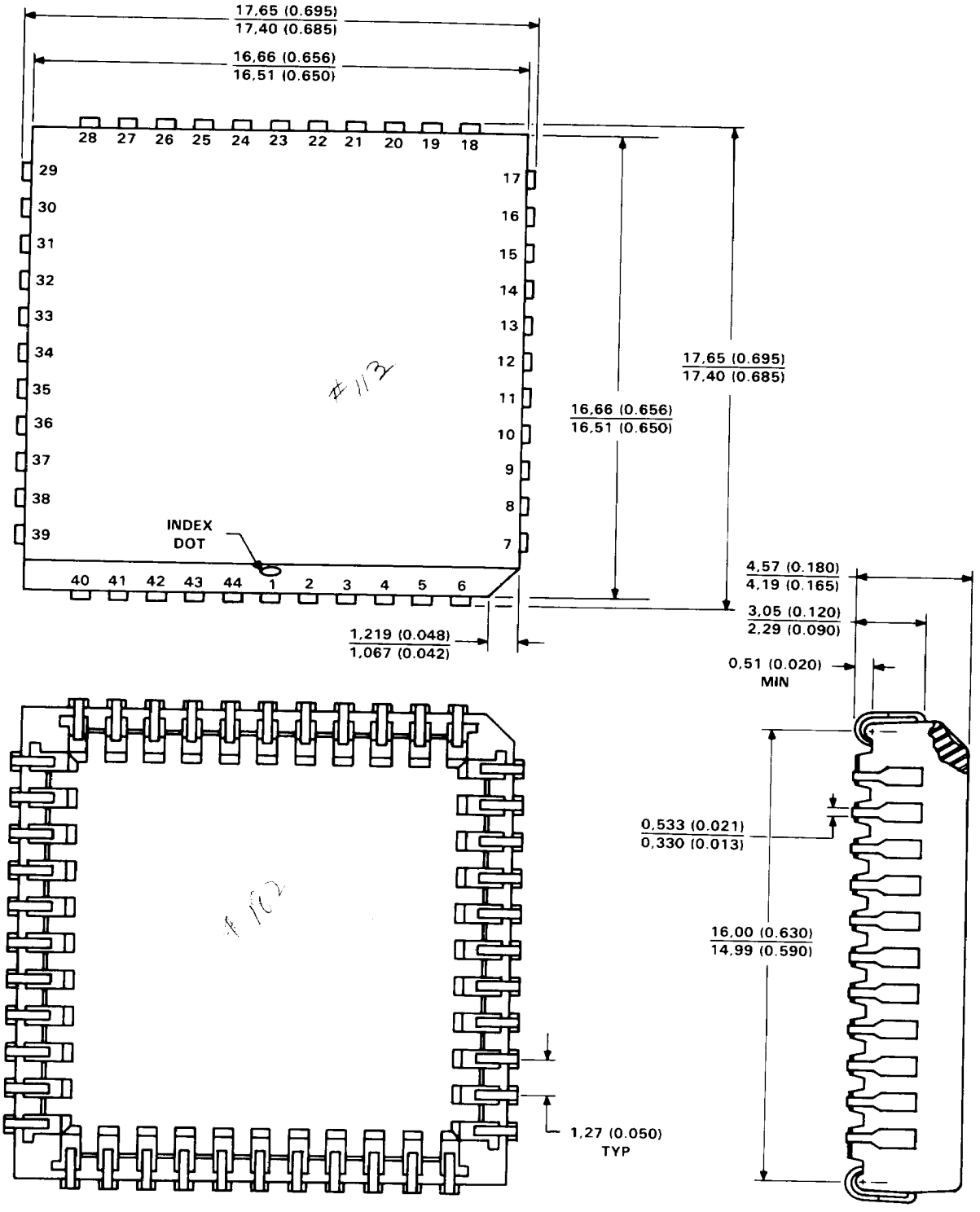
## MECHANICAL DATA

### 44-lead plastic chip carrier package




ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES